In-Package Wireless Communication with TSV-based Antenna

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I. Introduction

Network-on-Chip (NoC) has been shown to be the most viable alternative to an interconnect bus for the scalability of the system [1]. On-chip antennas, implementing wireless interconnects, are introduced for improved scalability of NoCs in [2]. On-chip wireless links offer improved network performance due to long distance communication, additional bandwidth, and broadcasting capabilities of antennas. The most prominent on-chip antenna designs are the planar log-periodic and meander which have a surface-propagation of the EM waves of the antenna. The main detriment of these antennas, and surface-propagation in general, is the poor signal attenuation (i.e. path loss) even at small distances of 5mm. This work challenges the on-chip antenna design conventions, and pushes toward a Through-Silicon Via (TSV)-based antenna design called `TSV_A` that establishes wireless communication through the silicon substrate medium with only a 3 dB loss over a 30mm on-chip distance.

II. Design of TSV Antenna

The design of the proposed antenna is based on a typical disc-loaded monopole antenna. A TSV acts as the main radiating part of the monopole antenna: A novel on-chip antenna design labeled `TSV_A`, shown in Figure 1. A small optional cylindrical disc of copper at the bottom of the `TSV_A` can be used for impedance matching to improve the overall signal strength.

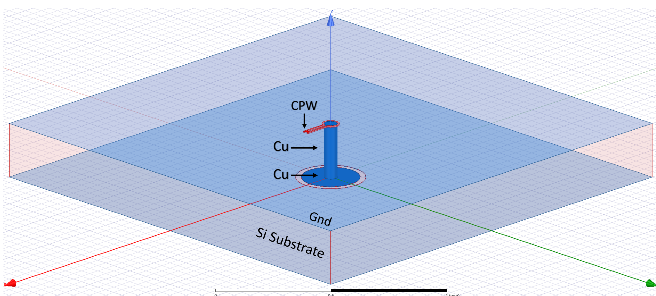

Fig. 1. The structure of the `TSV_A` in HFSS.

The `TSV_A` is placed inside the layer of silicon (Si) substrate. In HFSS simulations, the TSV material and cylindrical disc is selected to be copper (Cu), however any conductive material in varying TSV implementations could theoretically be used as the main radiating part of the monopole antenna. In simulations, the relative dielectric constant (ε_r) used for the Si substrate is 11.7.

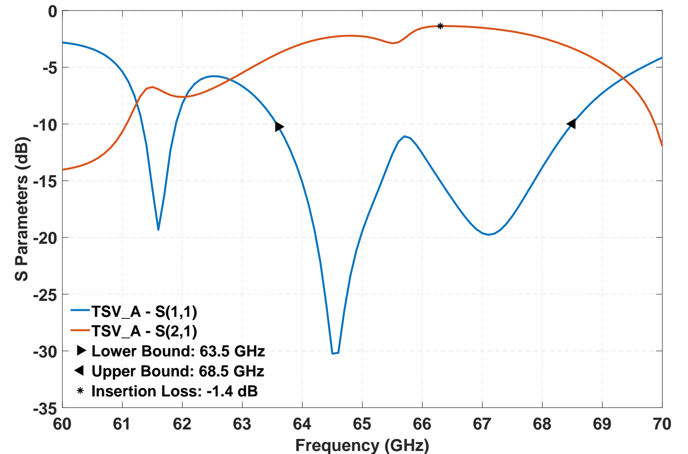

Fig. 2. S-parameters of `TSV_A` pair.

III. Evaluation of `TSV_A`

S-parameters describe the input-output relationship between antennas, characterizing the channel to identify the frequency and bandwidth of transmission. Return loss (S11) represents how much power is reflected from the `TSV_A` (lower is better). Insertion loss (S21) represents the power received at the second `TSV_A` (higher is better). S-parameters for a pair of `TSV_A` communicating at 5mm distance are shown in Figure 2. The `TSV_A` pair are communicating at a distance of 5mm and a bandwidth of 5 GHz can be achieved in the 63.5 to 68.5 GHz frequency range. The insertion loss (S21) in that range peaks at 1.5 dB and on average it is 2.3 dB. The insertion loss of `TSV_A` at greater distances (up to 30mm tested) remains $\approx$3 dB.

IV. Conclusions

This work proposes a novel communication infrastructure, utilizing TSVs for on-chip wireless communication. FEM simulations are performed to validate the operation of the TSV antenna (`TSV_A`). Simulation results indicate that the `TSV_A` is capable of transmission up to 30mm distance at a minimal insertion loss of $\approx$3 dB, which is a substantial improvement over current on-chip wireless antennas.

V. Related Works

The feasibility of on-chip wireless antennas is studied by K. Kim [3, 4]. Lin et al. [5] demonstrate fabricated (90nm–130nm technology) antennas to be fully operational. Yu et al. [6] propose (and fabricated in 65nm bulk CMOS process) an on-off keying (OOK) transceiver which consume only 1.2 pJ/bit at a data rate of 16 Gb/s operating at 60 GHz. Substrate propagation dipole antennas are achieved by placing vertical undoped silicon layers connected to the substrate underneath, in [7]. These vertical layers adversely affects the floorplan of active devices on chip (limiting utilization and prohibiting the use of sides).

VI. Supplemental Material

An illustrative (not to scale) representation of two `TSV_A` communicating is shown in Figure 3. The FEOL and BEOL layers are compliant with common manufacturing processes as well as modern ASIC flow, with no influence on those processes, other than the TSVs reserved for wireless communication. The silicon substrate layer under the active layer acts as a waveguide for the signal. Fabrication of the `TSV_A` follows the standard 3D-IC procedures for typical TSVs.

Path loss analysis of the `TSV_A` is performed in Section VI-A. Analyses of the interference between `TSV_As`, including those with TSVs, are presented in Section VI-B. Feasibility study of `TSV_A` is detailed in Section VI-C.

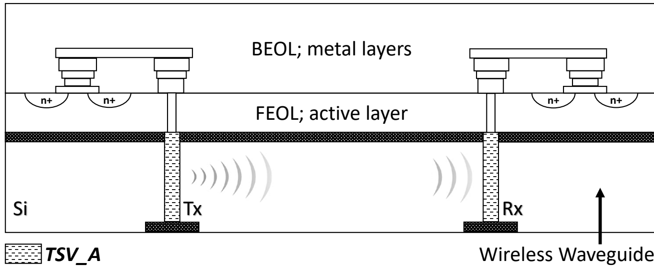

Fig. 3. Illustration of die cross-section with 2 TSV_As.

A. Path Loss Analysis

Path loss is a major component in the characterization of transmission distance and power consumption, and represents the reduction of the input power as the EM field propagates through the substrate. Path loss analysis is performed for the `TSV_A` and compared against the planar log-periodic [8] and meander [9] antenna. The results of the evaluation are shown in Figure 4. The two `TSV_As` (Tx and Rx) are placed at increasing distances (1.25mm–30mm) from each other and the transmission coefficient (S21) is recorded from the HFSS FEM simulations. The `TSV_A` has an almost constant and very low *3 dB* path loss due to the undoped silicon substrate layer acting as a wireless waveguide for the signal. The planar log-periodic and meander antennas suffer from exponential increase in path loss (up to 40 dB for the meander and up to 35 dB for the log-periodic antennas) due to the surface-propagation of the EM field. Improved path loss leads to several benefits, including: 1) The removal of low-noise amplifiers (LNAs), 2) low and constant power consumption, and, 3) increased `TSV_A` position flexibility during design-time.

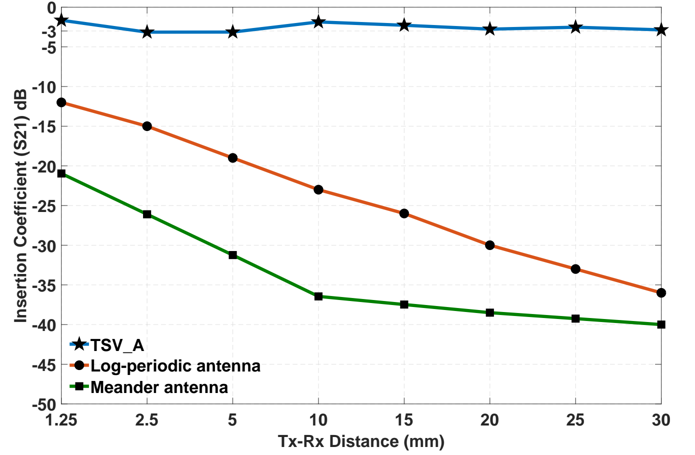

Fig. 4. Transmission coefficient (S21) versus distance.

B. `TSV_A` Interference from TSV

In Figure 5, two `TSV_As` are placed on the same board at a distance of 6mm. Multiple randomly placed TSVs are added between the `TSV_As` to quantify the interference caused from other TSVs in the system. Multiple structures are evaluated including a sweep of 1 to 4 TSV rows for 3-D memory applications, and additionally one hundred other structures with randomly placed TSVs on the board, as shown in Figure 5. Return loss (S11) and insertion loss (21) for all obstructions are shown in Table I. All TSVs have a radius of 20µm and are equally spaced at 225µm in the row structure case. The return and insertion loss of the 100 randomized placements are averaged together. Without any obstruction, the `TSV_As` has a return loss of 16 dB and insertion loss of 2.2 dB. With 3 or 4 TSV rows of obstruction, the minimum return and insertion loss are 8.5 dB and 17 dB, respectively.

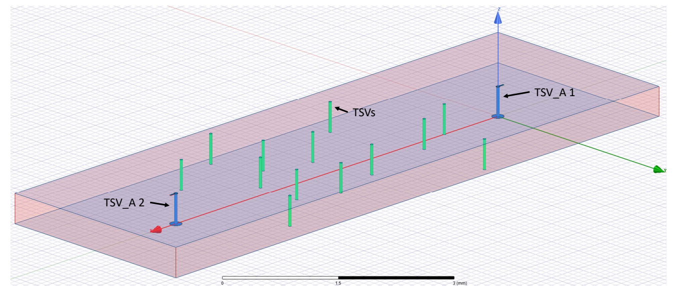

Fig. 5. `TSV_A` pair obstructed by randomly placed TSVs.

The average return and insertion loss of the `TSV_As` with the randomized TSV obstructions are 15.5 dB and 6.6 dB, respectively. `TSV_A` is shown to operate with additional TSVs in the silicon substrate layer, and even in the worst-case scenario it performs better than the planar log-periodic [8] and meander [9] antennas, at ≈20 dB to ≈30 dB at 6mm distance,

TABLE I. TSV impact on TSV_A performance.

Obstruction	Return Loss (S11)	Insertion Loss (S21)
None	16 dB	2.2 dB
1 Row TSV	12 dB	7 dB
2 Row TSV	12 dB	12 dB
3 Row TSV	8.5 dB	16 dB
4 Row TSV	8.5 dB	17 dB
Random	15.5 dB	6.6 dB

without any interference. For optimal signal performance, the substrate layer can be dedicated only to the TSV_As for RF communication. If the silicon substrate layer cannot be dedicated to the TSV_As, guidelines can be developed for floorplanning to minimize interference between TSV_As and typical TSVs.

C. Feasibility Study of TSV_A

The feasibility of the aspect ratio of 5:1 selected in this work for the TSV_A size is demonstrated in [10, 11]. For example, DRIE [11] is capable of forming a wide range of via holes up to an aspect ratio of 100:5. In addition, the research community has investigated the process robustness in-depth, sweeping the via dimensions from 3-80 μm wide and 45-160 μm deep in in 150mm and 200mm wafers [10]. There is active research in the manufacturing of TSVs for 3D ICs and interposers. The TSV_As benefit from these packaging and manufacturing innovations.

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