Two-Element Antenna-Active Phase Shifter Packaging at 77 GHz

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***Abstract*—This work presents a low cost and wire-bonded active phase shifter chip to RF circuitry on PCB board packaging for implementing a two-element phased array antenna at 77 GHz. The 1.5 mm × 1.1 mm chip is embedded in RO3003 PCB board and its GSG ports are wire-bonded to CPW lines that are expanded to feed the patch antenna on the PCB board. A low loss CPW to microstrip line transition is designed to exploit and transmit the signal from the GSG pads on the chip to the microstrip line on the PCB. The beam of the two-element array can be steered between ±20° by controlling the DC bias voltage of the active phase shifter chip.**

***Index Terms*—77 GHz patch antenna, active phase shifter, wire bonding.**

I. Introduction

mm-wave frequency radars and especially 77 GHz automotive radar are being developed with new features such as beam steering, high precision, automatic calibration, etc. Connecting different modules at lower frequencies may be easy, but when the frequency is increased, the connections are going to be more sensitive and in some cases impossible. At higher frequencies, the size and accuracy of the connections have significant effects on transmitted/received signals. Development of technology created various methods of packaging such as embedded wafer level ball grid array (eWLB) package, flip-chip and wire bonding chip to PCB. For instance, a 77 GHz automotive radar receiver with 16 elements and ±50° beam steering capabilities is packaged using bond wire technique for integrating the single chip on the board [1]. In this paper, a two-element antenna array that is accompanied by LNA/phase shifter chips [2] (A, B in Fig. 1) and DC/RF circuit on the RO3003 board are packaged using wire bonding technique. First, the chips are placed in a rectangular cut hole in the middle section of the CPW (coplanar waveguide) line and then the GSG pads of the chip are wire-bonded to the signal and ground metals of the CPW line for RF connection and DC bias lines to DC pads of the chip to bias the active phase shifter circuitry. The CPW line is connected to the MS (microstrip) line at both sides using two transition sections. MS lines are connected to two microstrip patches on one side and a Wilkinson power combiner at the other side. The whole system is designed and measured for steering the beam along y-axis at 77 GHz.

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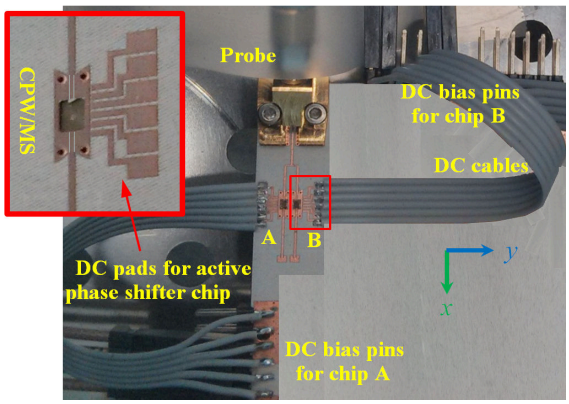


Fig. 1. 77 GHz two-element phased-array.

II. Wire-Bonding

In order to carry out the signal from active the phase shifter chip to the circuitry on the PCB, the low cost wire bonding is preferred. As shown in Fig. 2, the thin (h = 130 μm) RO3003 board with dielectric constant of ε_r = 2.8 (at 77 GHz) and 17 µm copper cladding is laminated on a thicker (500 μm) FR4 PCB to increase the mechanical strength of the board and hold/fix the chip. The chip is placed in a rectangular hole with 350 μm height (the Si chip height) which is etched on the board. However, the epoxy thickness can cause the chip surface to be located at higher level (Δy) with respect to the board surface. This Si chip which has a gain of 10 dB will provide 0-360° phase, by changing the DC bias voltages, to steer the array beam. The Si chip is an IQ vector modulator type phase shifter.

The GSG pads on the chip are wire bonded to three tracks of 50 Ω CPW on the RO3003 board.

Although the wire bond interconnection is low cost compared to the other methods such as flip-chipping and eWLB, this method has considerable insertion loss at mm-wave frequencies due to high inductance and the radiation from the bond wires. However, decreasing the height of bond and bending it closer to the surface metal ground (the signal can couple to the surface metal and form a transmission line) can alleviate the problem by some degree. To investigate the effect of bonding height and length (h_{bond} and ℓ_{bond} in Fig. 3)

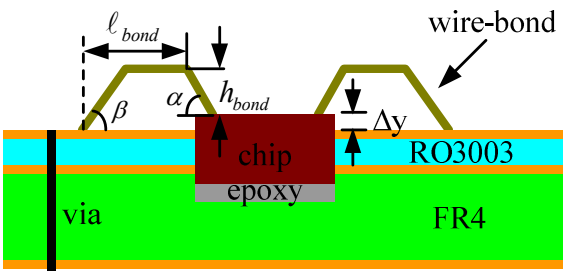


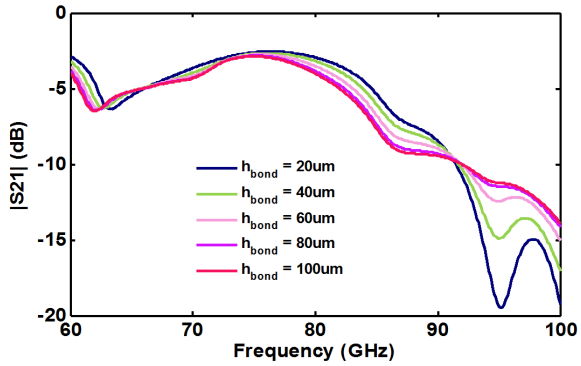
Fig. 2. Cross-sectional view of embeded the chip in the hole on PCB and wire bonded to CPW line on RO3003.

and have an idea about the insertion loss of the used wire-bonding technique, some simulations are done.

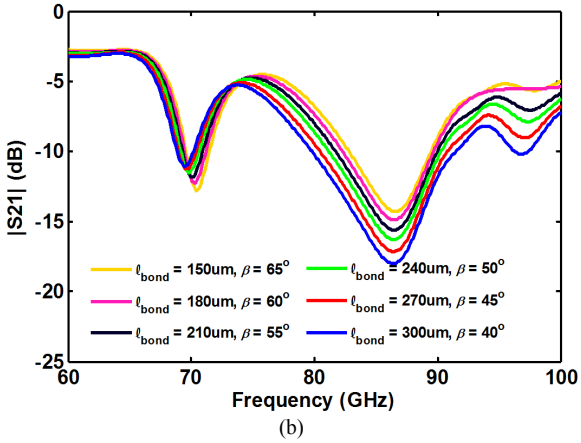
The bond height (h_{bond}), distance (ℓ_{bond}), chip height from the PCB level (Δy) and rising (α), falling (β) angles of the gold wire with diameter of 20 μm are shown in Fig 2.

To show the total loss of the two bonds, the simulations are performed for a structure with two bonding connections at both input and output of the chip. The chip is modeled with its actual size (1.1 × 1.5 mm^2), and a 50-ohm MS line between two GSG pads on the 11.4 μm thick SiO_2.

To see the effect of signal trace width of CPW in the wire-bond insertion loss, several 50-ohm CPW lines were designed and simulated. However, the etching resolution for the used PCB prototyping machine (LPKF laser) was limited to 50 μm, which can be suitable to produce a 50-ohm CPW line



(a)



(b)

Fig. 3. Simulated insertion loss of two wire bond sets for different (a) heights and (b) lengths of bonds.

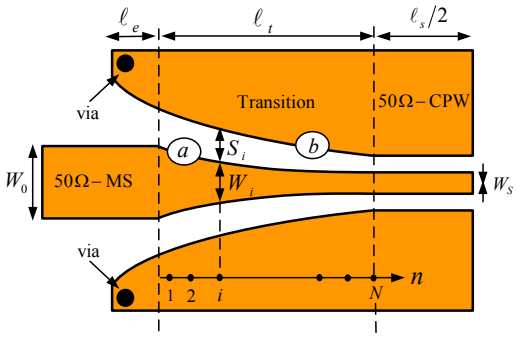


Fig. 4. Schematic of Klopfenstain-tapered transtion from MS to CPW line.

with signal trace width and gap spacing of W_s = 200 μm and S = 50 μm, respectively.

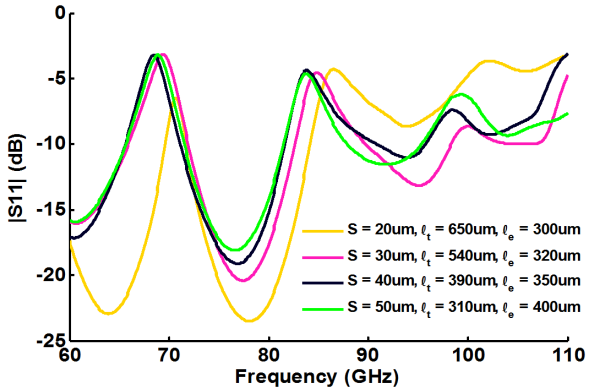
The simulation results show that increasing the width of signal line increases the wire-bond insertion loss. Nevertheless, the electromagnetic field of RF signal on wire bonds can couple to the underneath metal and behave as a transmission line, which prevents much more radiation loss while reducing the spacing between them.

Changing h_{bond} from 20 μm to 100 μm presents a very small variation in bonding loss at 77 GHz (Fig 3 (a)). During the simulation, the other parameters are α = 40°, β = 65°, Δy = 80 μm, ℓ_{bond} = 200 μm. Since the angles α and β are fixed during the process, variation of the bonds total length does not cause significant changes. Apparently, increasing the bond distance (ℓ_{bond}), increases the bond length and hence insertion loss. The simulations in Fig. 3. (b), for the swept ℓ_{bond}, are to specify the range of the insertion loss which is imposed by performing different distance bonding in practice. In this simulation, α = 40°, Δy = 130 μm, and h_{bond} = 40 μm.

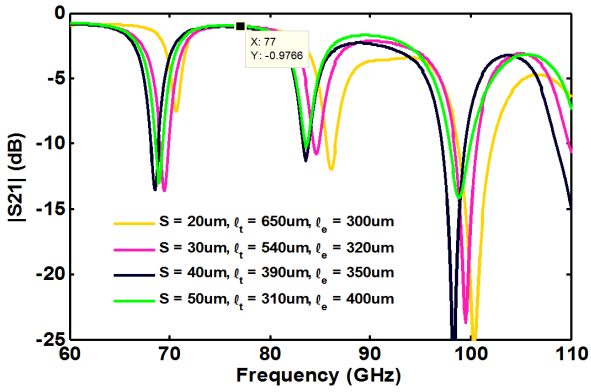
The measurement of various implemented wire-bonds show that the parameters h_{bond} and ℓ_{bond} are laying in the range of 30 to 50 μm and 180 to 250 μm, respectively. Therefore, the simulated insertion loss can stay in the range of 5-7.5 dB at 77 GHz.

III. Via-Less CPW/MS Transition and Via Effect

The chip signal's connection is provided using CPW lines, while the patch antennas and feed are supported using MS lines. These CPW and MS transmission lines are required to be connected to each other with a transition section, which insertion loss should be low. Hence, the Klopfenstein impedance matching method [3] is applied for tapering the MS line width (W_0 = 318um) to signal trace of CPW line W_s, while $W_0 > W_s$ (Fig. 4). This new application of the Klopfenstein tapering is employed for the first time in the design of CPW-to-MS transition. To form the transition section, the MS-line impedance of width W_s (CPW signal trace width) is calculated by considering only the signal line of CPW. Then, the 50 ohm MS line (W_0) is tapered (Klopfenstein method) to the MS line with trace width of W_s. Afterward, the gap spacing (S_i) around the CPW line is calculated in the transition part by keeping the CPW line impedance at 50 ohm. This process is performed by dividing the transition part to N points, as shown in Fig. 4. At point $i = N$, W_i approaches to $W_N = W_s$. Here, the

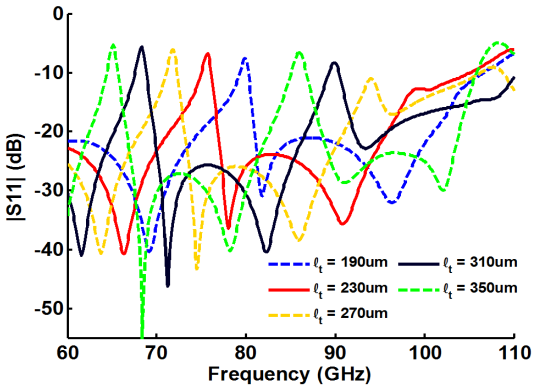


(a)

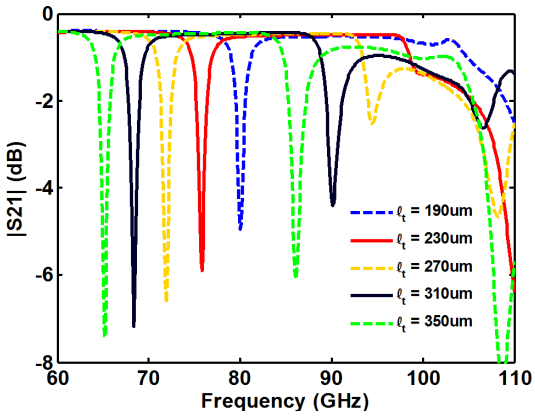


(b)

Fig. 5. The (a) return loss and (b) insertion loss for back-to-back via-less MS-to-CPW.



(a)



(b)

Fig. 6. The (a) return loss and (b) insertion loss for various transition lengths of back-to-back MS-to-CPW with four vias at the ends of ground plates.

obtained N points at both curves *a* and *b* are interpolated using a 5th order polynomial to have a smooth transition. The ground plates are extended by the length of ℓ_e, as shown in Fig. 4, to improve the circuit matching and couple the MS ground to these plates. To avoid the complexity in fabricating vias, the designs are done without vias. Nevertheless, due to space limitation, two vias are embedded at the outer edges of the ground plates to use them as the DC ground of the chip. Moreover, these vias can improve the transition matching at wideband by easing the ground signal coupling at RF frequencies, and the structure can be tuned by changing the transition length (ℓ_t).

Some via-less back to back connected MS-to-CPW line designs were performed to connect a 50 Ω MS to a 50 Ω CPW with different gap spacing (S). The magnitude of S_{11} and S_{21} are presented in Fig. 5. Each case is optimized for a maximum return loss at 77 GHz, with respect to the transition length ℓ_t and extended ground plates length ℓ_e. Quantities ℓ_t and ℓ_e are shown in Fig. 4.

The simulations in Fig. 5. are done for two similar back to back connected MS-to-CPW transition with ℓ_s = 3 mm. The 10 dB return loss bandwidth is more than 10 GHz and will be larger as the gap spacing (S) is reduced. The simulations show an insertion loss better than 1 dB at 77 GHz, as shown in Fig. 5. (b). As the S is increased, the transition length is reduced and extended length is increased. In a 50 Ω CPW line, reducing S will increase the value of signal trace width (W_s) and hence connecting a shorter W_s to a 318 μm (trace width) 50-ohm MS line needs more transition length. On the other hand, the shorter transition lengths are compensated with longer ℓ_e to make the matching good around the operating frequency.

The overall width of the CPW line including the signal trace width, two gap spacings and two ground plates' widths is fixed to 1.7 mm.

The via-less design is modified by inserting vias at the shown locations in Fig. 4 and reducing the values of ℓ_t and ℓ_e. The effect of the transition length (ℓ_t) in tuning the frequency is shown in Fig. 6. for S = 50 μm. In the simulations of the Fig. 6, ℓ_t is changed between 190 to 350 μm, by setting ℓ_s = 4 mm, ℓ_e = 200 μm and a total width of CPW (W_s+2S+2G) equal to 1.7 mm. The results show that the vias widen the bandwidth (15 GHz 10 dB bandwidth) and reduce the insertion loss. As expected, increasing ℓ_t causes a shift to lower frequencies. Simulated results, show ℓ_t = 270 μm is suitable for the desired frequency band.

IV. Fabricated Two-Element Radar Front-End

The active phase shifter chip is integrated with the circuit on the PCB board to form the 2-element phased array receiver front end at 77 GHz, as shown in Figs. 1 and 7. The spacing

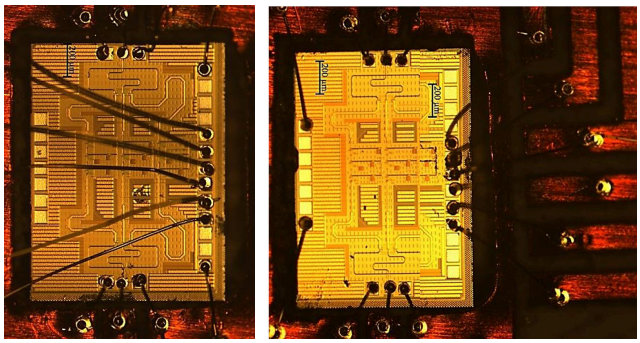


Fig. 7. Microphotograph of the wire-bonded chips A (left) and B (right).

between patch antennas is 2 mm. Since the width of the CPW structures is 1.7 mm, the CPWs of chip A and B are separated by a 300 μm gap. Due to space limitation between the chips A and B, their DC traces are places at left and right (Fig. 1 (a)) sides on PCB, while the DC pads on the chip [2] is located on its right side. Hence, the DC bonds for the chip A cross over (left picture in Fig. 7) the chip to be connected to corresponding pads on the chip. Wire bond interconnections for chips A and B with the specified antenna position are shown in Fig. 7. As was measured for the integrated chip, the total insertion loss fluctuated around 0 dB (containing the chip gain, bonding and transition losses). Since the measured gain of a single patch antenna is 5 dBi at 77 GHz, a maximum gain of 8 dBi is expected from the 2-element array.

The measured array gains in H-plane of the patch antenna (*yz*-plane) for different bias voltages are shown in Fig. 8. The beam steering is performed for confined number of angles. Since the array is composed of only two antennas, the array factor beam width is wide and in the case of phase diffrence between elements, the array factor maximum is dominated by the patch antenna beam maximum. Therefore, changing the phase difference between the antennas imposes only some difference in the gain pattern shape, and the maximum position does not change significantly. The measured beam pattern gain is around 6.5 dBi which is 1.5 dB lower than the expected value. This difference can be due to the long transmission lines which increase the line loss and radiation and higher wire bond loss. During the measurements, the DC base control voltages of the used LNAs are set to 1.5 V and collector voltages are changed from 1 to 2 V with the step of 0.2 V. The beams in Fig. 8 are obtained using the bias voltages displayed in Table I. Because of the high DC current flow in LNA 3 of Chip B, only two LNAs of this chip are biased. Due to lower resolution of the array beam which is dominated by the single patch radiation pattern, the other combinations/collector voltages have very similar beams to those in Fig. 8 and are not shown here.

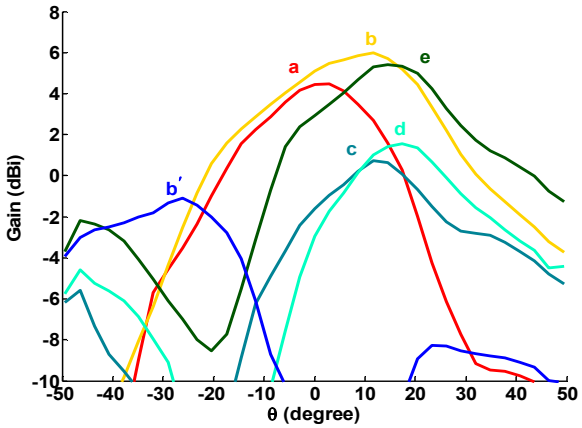


Fig. 8. Beam-steering measured gain at 77 GHz for the 2-element radar receiver.

TABLE I
DC BIAS VOLTAGES OF CHIPS A, AND B FOR STEERING THE BEAM TO DIFFERENT POSITIONS

Beam Position	Collector DC Bias Voltages of Chip A and B				
	Chip A			Chip B	
	LNA 1	LNA 2	LNA 3	LNA 1	LNA 2
a	2.00	2.00	—	1.60	2.00
b	2.00	—	2.00	2.00	1.00
c	1.00	—	2.00	2.00	2.00
d	1.20	—	2.00	2.00	2.00
e	1.60	—	2.00	2.00	2.00
b´	1.00	—	2.00	1.00	2.00

Values are in volt.

V. CONCLUSIONS

A three way active phase shifter chip was integrated to RF circuit on the RO3003 board using wire bonding technique. The insertion loss that can be obtained from bonding was studied in different simulations. The via-less transition from MS-to-CPW based on Klopfenstein impedance matching was introduced and used to connect chips to antennas and power combiner. A two-element radar receiver front-end was steered in the H-plane beam between -20° and 20°. The array suffers from poor resolution due to low number of array element that cause the widebeam array factor.

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