A 5-13 GHz 6-Bit Vector-Sum Phase Shifter with +3.5 dBm IP1dB in 0.25-μm SiGe BiCMOS

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***Abstract*—This paper presents a wideband vector-sum phase shifter (VSPS) with high phase resolution and high input-referered 1 dB compression point (IP1dB) which covers the full 360° phase range with 5.6° phase steps between 5-13 GHz in a commercial 0.25-μm SiGe BiCMOS technology. A transformer balun and an RC polyphase filter (PPF) are implemented for in-phase and quadrature phase (I/Q) reference vector generation while the desired phase states are generated by an adder stage where the amplitudes of the I/Q reference vectors are manipulated with digitally controlled variable gain amplifiers (VGAs). The measured root mean square (RMS) phase error of the VSPS is <2.8° between 7.4-10.3 GHz and <5.6° between 5.4-11.9 GHz with a measured average insertion loss >7.8 dB. Thus, the VSPS achieves 6-bit phase resolution. IP1dB for the 1^{st} state of the VSPS at 10 GHz is measured to be +3.5 dBm. Overall chip size of the VSPS IC is only 1.22×0.59 = 0.71 mm^2, excluding the RF and the DC pads.**

***Index Terms*—Vector-sum phase shifter, active phase shifter, transformer balun, I/Q network, VGA, SiGe BiCMOS, phased array.**

I. Introduction

There are numerous applications for integrated electronic phase shifters such as measurement equipments, amplifier linearization systems, image rejection receivers, phase-locked loops, multiple-input multiple output radio links and phased arrays. As the number of applications for the integrated electronic phase shifters grow, so does the motivation for improving their overall performance parameters such as the phase resolution and accuracy since the overall performance of the systems are directly related to quantization loss levels of the implemented phase shifters.

Traditionally the integrated electronic phase shifters have been implemented as passive phase delay networks such as switched transmission lines and switched high-pass and low-pass filters [1]–[5]. Even though the passive phase shifter topologies can provide excellent large signal handling capabilities with nearly zero power consumption, their narrowband performance along with the total physical size and insertion loss levels which are increasing with the desired high phase quantization levels make them an unfavored choice to be implemented in the modern systems [6], [7].

When compared to passive phase shifter topologies, active phase shifter topologies such as vector-sum architectures, sometimes referred as vector-modulators provide better phase quantization levels in smaller chip sizes [8]–[10]. Unlike the passive phase shifter topologies, increasing the phase quantization levels in the vector-sum phase shifters (VSPS) do not increase the overall chip size but only increases the complexity of the digital control circuitry [11]–[14].

This work focuses on the important design considerations for the VSPS architectures in order to achieve very high levels of phase quantization levels or phase resolution in a very compact chip size while also achieving high input linearity which is also a known issue for the VSPS architectures. Section II describes the implemented VSPS and specific circuit level descriptions of its building blocks in detail. The measurement results of the VSPS are discussed in Section III.

II. Circuit Design

A. Vector-Sum Phase Shifter Architecture

VSPS architectures take advantage of the in-phase and quadrature phase (I/Q) signals in order to generate the desired phase states rather than using true-time or synthetic delay elements as the passive phase shifter topologies. In theory, any phase state can be generated with a linear combination of two I/Q reference vectors which are 90° apart from each other given that the magnitude and polarity of reference vectors can be controlled. A typical VSPS consists of an I/Q reference vector generation stage and an adder stage where the magnitude of the each reference vector is decided in order to generate the desired phase state after the vector-summation operation.

B. Transformer Balun

The essential function of the transformer balun presented in the Fig. 1 is to provide single-ended-to differential signal conversion for the I/Q network while providing a 50-Ω input matching for the measurement devices and previous system blocks. Thus, amplitude balance and a desired phase imbalance of 180° between the outputs of the transformer balun needs to be preserved in the desired bandwidth in order to ensure the performance of the I/Q network. The reason of implementing a transformer balun instead of a CB-CE pair type or an emitter-coupled differential amplifier type active balun is to

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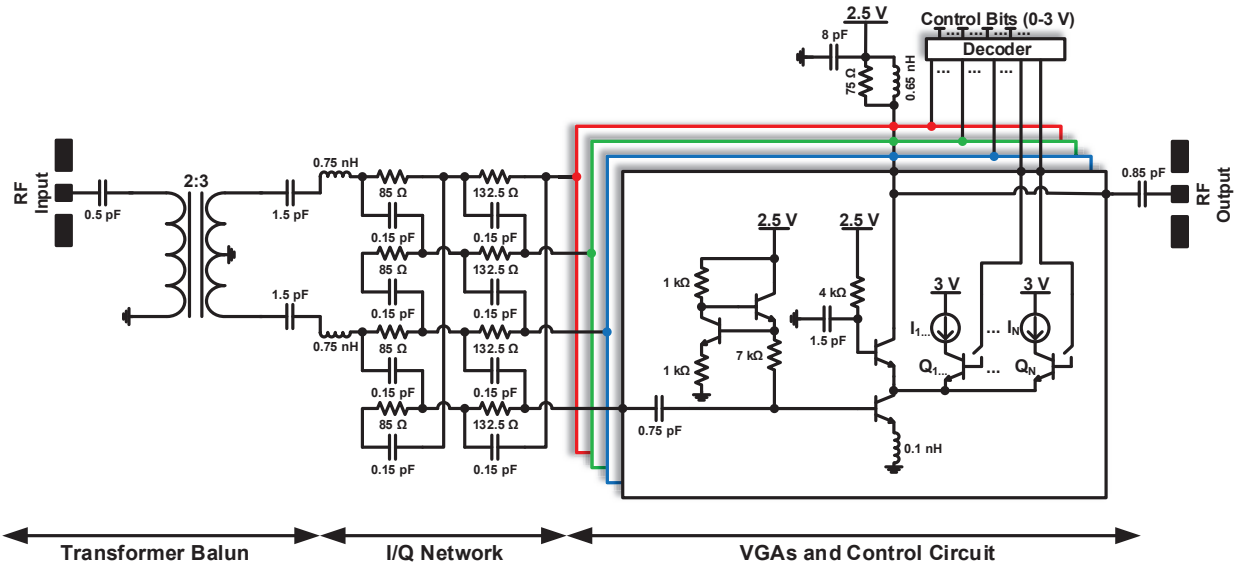

Fig. 1. Detailed schematic of the implemented vector-sum phase shifter

increase the overall linearity performance of the VSPS while also minimizing the total chip area.

The single-ended-to-differential signal conversion is achieved by grounding one of the windings of the transformer at the electrical center or center tap as shown in Fig. 1. EM simulations of the transformer balun are realized in ADS Momentum in order to further insure the performance. Measurement results for the standalone transformer balun suggests that the amplitude imbalance between the respective outputs of the transformer balun is $<$1.1 dB while the insertion loss is $>$1 dB and the undesired phase imbalance between the outputs is $<1.6^\circ$ between 5 and 13 GHz.

C. I/Q Network

I/Q networks are used to generate the orthonormal reference vectors for the interpolation operation of the VSPSs. An ideal I/Q network should be able to maintain the amplitude balance and the desired phase relationships between its outputs over the desired bandwidth. Considering that the accuracy of the generated phases are sensitive to any unexpected amplitude and phase errors between the I/Q reference vectors, the I/Q network that will be implemented in the VSPS should be designed with great care in order to ensure the high phase resolution and bandwidth of the VSPS.

In order to generate the I/Q reference vectors accurately over a wide frequency range as desired, a constant-phase type second-order RC polyphase filter (PPF) is implemented in the VSPS as presented in Fig. 1. Phase difference between the $I_\pm$ and $Q_\pm$ outputs of a constant-phase type RC PPF is exactly 90° at all frequencies while the amplitude balance between the $I_\pm$ and $Q_\pm$ outputs is achieved at $\omega_{ppf} = 1/R_{ppf}C_{ppf}$. Simulation results suggest that the undesired amplitude imbalance between the $I_\pm$ and $Q_\pm$ outputs of the RC PPF that is implemented in the VSPS is $<$1.5 dB while the insertion loss is $>$12 dB between 5 and 13 GHz.

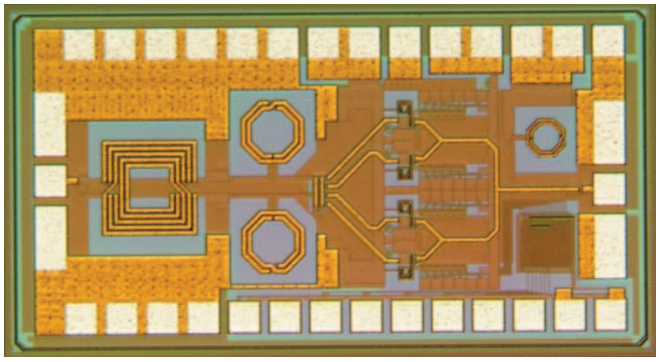

Fig. 2. Chip photo of the implemented vector-sum phase shifter

D. VGAs and Control Circuit

Adder stage of the VSPS, which is the final stage, is implemented by four identical variable gain amplifiers (VGAs), one VGA for each I/Q reference vector and a decoder based digital control circuit for the VGAs in order to manipulate the amplitude weighting of each I/Q reference vector for the vector-summation operation and generate the desired phase states as presented in Fig. 1.

Cascode amplifiers with current-steering transistors are implemented as VGAs as presented in Fig. 1 where $I_1, ..., I_N$ are different amounts of currents that are mirrored from a current source over the collectors of the $Q_1, ..., Q_N$ HBTs that are acting as switches which are controlled by the decoder

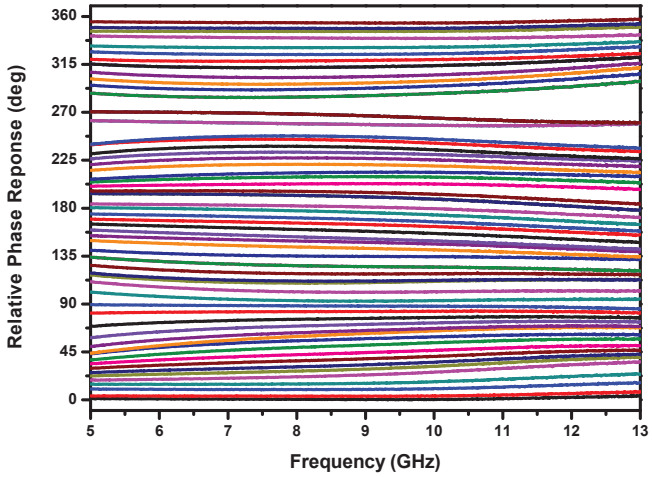

Fig. 3. Measured relative phase response of the vector-sum phase shifter when the input power level is -20 dBm

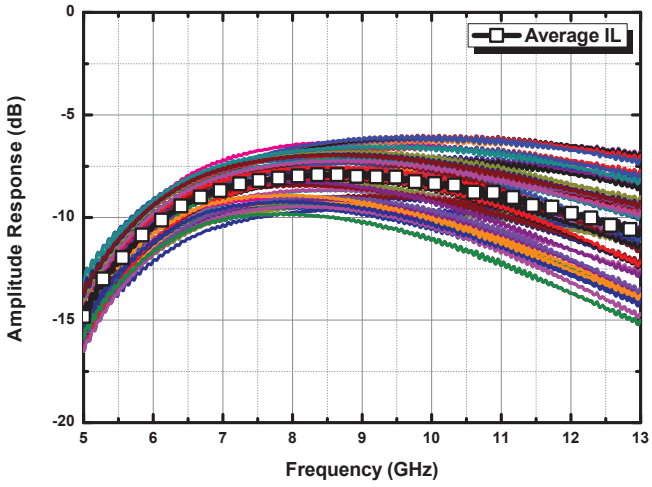

Fig. 4. Measured amplitude response of the vector-sum phase shifter when the input power level is -20 dBm

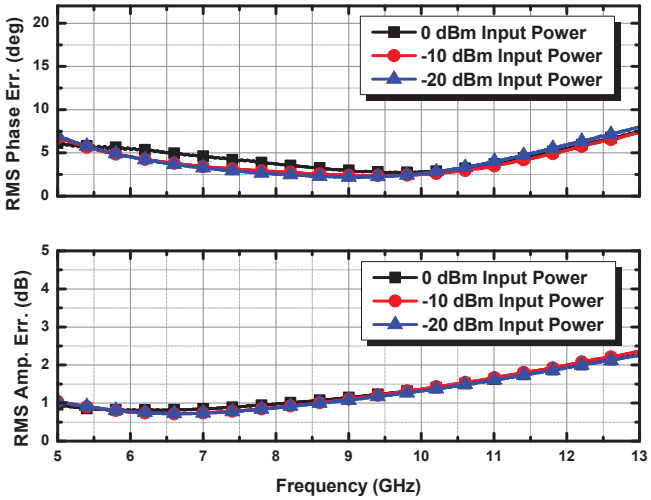

Fig. 5. Measured RMS phase and amplitude errors of the vector-sum phase shifter for different input power levels

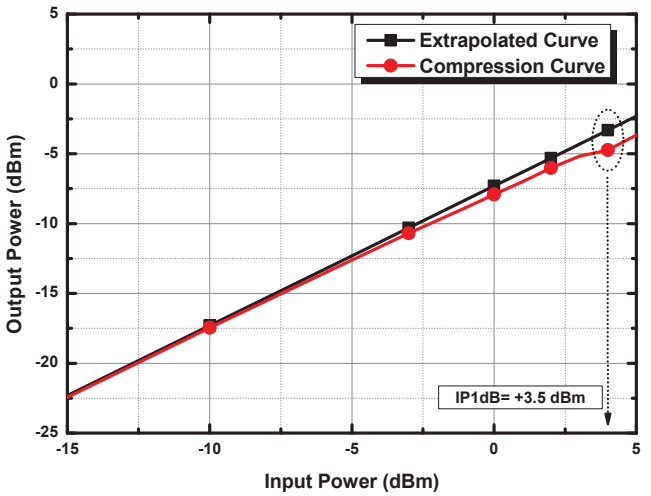

Fig. 6. Measured input-referred 1 dB compression point data for the first state of the vector-sum phase shifter

circuit for digitizing the current-steering operation. When the base of a "current-switch" HBT is set to the V_{dd} state by the decoder circuit, the amount of mirrored current to its collector is steered from the cascode amplifier. Thus, variable gain operation in order to manipulate the amplitude weighting of the corresponding I/Q reference vector is achieved. When the base of a "current-switch" HBT is set to the 0 V state by the decoder circuit, gain of the cascode amplifier does not change since the amount of steered current is zero. Amounts of the $I_1, ..., I_N$ currents and output states of the decoder circuit are decided by simulation results and $\theta_{desired} = \angle \tan^{-1}(Q_{o\pm}/I_{o\pm})$ formula while selecting a constant amplitude for the output of the vector-summation operation. Vector-summation operation between the $I_{\pm}$ and $Q_{\pm}$ reference vectors results in the desired phase states and the relationship between the output phase states and the control bit sequence is linear.

III. Measurement Results and Discussion

The VSPS is realized in the IHP SG25H3 0.25-μm SiGe BiCMOS technology where SiGe HBTs have f_T/f_{max} of 110/180 GHz. Fig. 2 presents the die photo of the fabricated chip. Overall chip size of the VSPS IC is only 1.22×0.59 = 0.71 mm^2, excluding the RF and DC pads.

S-parameters of the VSPS are measured on-chip with GGB Picoprobe ground-signal-ground (GSG) probes after a standard short-open-load-through (SOLT) calibration using the Rohde&Schwarz ZVL network analyzer. In order to investigate the performance of the VSPS at increasing input power levels, three different S-parameter measurements have been performed at -20, -10 and 0 dBm input power levels. Fig. 3 presents the measured relative phase response of the 64 different phase states generated by the VSPS between 5 and 13 GHz with 5.6° phase steps where the 1^{st} state is selected as

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

	[3]	[5]	[12]	[14]	This Work
Technology	0.18-μm SOI	0.13-μm SiGe BiCMOS	0.18-μm SiGe BiCMOS	0.25-μm SiGe BiCMOS	0.25-μm SiGe BiCMOS
Method	Switched-Filter Type	Switched-Filter Type	Vector-Sum	Vector-Sum	Vector-Sum
Frequency Band	8-12 GHz	8-12 GHz	6-18 GHz	8-12 GHz	5-13 GHz
Phase Resolution	5-bit	5-bit	5-bit	6-bit	6-bit
Phase Range	360°/11.2°	360°/11.2°	360°/11.2°	360°/5.6°	360°/5.6°
Phase Error (RMS)	$<$6.5°	$<$8°	$<$5.6°	$<$6.4°	$<$7.9°
Amplitude Error (RMS)	$<$0.5 dB	-	$<$1.1 dB	$<$2 dB	$<$2.2 dB
Insertion Loss (Ave.)	$>$9 dB	$>$20 dB	$<$ 19.5 dB (Gain)	$>$2.5 dB	$>$7.8 dB
Input P1dB	10 dBm	-	-39.5 dBm	-11 dBm @10 GHz	+3.5 dBm @10 GHz
Power Consumption	0 mW	$<$1 mW	61 mW	110 mW	90 mW
Chip Area	1.14$\times$0.78 mm^2*	1.8$\times$2.7 mm^2	1.2$\times$0.75 mm^2	1.87$\times$0.88 mm^2*	1.22$\times$0.59 mm^2*

* Excluding RF and DC pads

the reference state and the input power level is -20 dBm. Fig. 4 presents the measured amplitude response of the VSPS at -20 dBm input power level where the average insertion loss is $>$7.8 dB between 5 and 13 GHz. The measured RMS phase and amplitude errors of the VSPS at -20, -10 and 0 dBm input power levels are presented at Fig. 5. As the measurement results suggest, RMS phase and amplitude errors of the VSPS between 5 and 13 GHz do not vary in the range of -20 to 0 dBm input power levels. The measured RMS phase error of the VSPS is $<$2.8° between 7.4 and 10.3 GHz and $<$5.6° between 5.4 and 11.9 GHz. The measured RMS amplitude error is $<$1 dB between 5 and 8.6 GHz and $<$2 dB between 5 and 12.5 GHz. Measured input return loss is $>$10 dB between 5 and 13 GHz and output return loss is $>$10 dB between 8.7 and 12 GHz during the 64 different states. Measurement results also show that the isolation between the input and output of the VSPS is $>$65 dB during different states. Lastly, measurement for the input-referred 1 dB compression point (IP1dB) of the VSPS is done by using the Agilent E4417A power meter and resulted in +3.5 dBm at 10 GHz for the 1^{st} state of the VSPS as presented in the Fig. 6. Overall power consumption of the VSPS is 90 mW.

IV. CONCLUSION

This paper has demonstrated a 5-13 GHz 6-bit VSPS in a commercial 0.25-μm SiGe BiCMOS technology which achieves +3.5 dBm IP1dB in only 1.22$\times$0.59 = 0.71 mm^2 chip area. Measurement results suggest that the implemented VSPS architecture is a very good candidate to be implemented in cost-effective and multi-band modern systems that require high phase resolution from phase shifters in a wide frequency range along with high input linearity.

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