SiGe BiCMOS ICs for X-Band 7-Bit T/R Module with High Precision Amplitude and Phase Control

By

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SiGe BiCMOS ICs for X-Band 7-Bit T/R Module

with High Precision Amplitude and Phase Control

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with High Precision Amplitude and Phase Control

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Keywords: Phased Array Radar, T/R Module, SiGe BiCMOS, Attenuator, SPDT switch, Low Noise Amplifier

Abstract

Over the last few decades, phased array radar systems had been utilizing Transmit/Receive (T/R) modules implemented in III-V semiconductor based technologies. However, their high cost, size, weight and low integration capability created a demand for seeking alternative solutions to realize T/R modules. In recent years, SiGe BiCMOS technologies are rapidly growing their popularity in T/R module applications by virtue of meeting high performance requirements with more reduced cost and power dissipation with respect to III-V technologies. The next generation phased array radar systems require a great number of fully integrated, high yield, small-scale and high accuracy T/R modules. In line with these trends, this thesis presents the design and implementation of the first and only 7-Bit X-Band T/R module with high precision amplitude and phase control in the open literature, which is realized in IHP 0.25µ SiGe BiCMOS technology.

In the scope of this thesis, sub-blocks of the designed T/R module such as low noise amplifier (LNA), inter-stage amplifier, SiGe Hetero-Junction Bipolar Transistor (HBT) Single-Pole Double-Throw (SPDT) switch and 7-Bit digitally controlled step attenuator are extensively discussed. The designed LNA exhibits Noise Figure (NF) of 1.7 dB, gain of 23 dB, Output Referred Compression Point (OP_{1dB}) of 16 dBm while the inter-stage amplifier gives measured NF of 3 dB, gain of 15 dB and O_{P1dB} of 18 dBm. Moreover, the designed SPDT switch has an Insertion Loss (IL) of 1.7 dB, isolation of 40 dB and OP_{1dB} of 28 dBm. Lastly, the designed 7-Bit SiGe HBT digitally controlled step attenuator demonstrates IL of 8 dB, RMS attenuation error of 0.18 dB, RMS phase error of 2° and OP_{1dB} of 16 dBm.

The 7-Bit T/R module is constructed by using the sub-blocks given above, along with a 7-Bit phase shifter (PS) and a power amplifier (PA). Post-layout simulation results show that the designed T/R module exhibits a gain of 38 dB, RMS phase error of 2.6°, RMS amplitude error of 0.82 dB and Rx-Tx isolation of 80 dB across X-Band. The layout of T/R module occupies an area of 11.37 mm^2.

X-Band Yüksek Hassasiyetli Faz/Genlik Kontrollü 7-Bit Alıcı/Verici Modülü için SiGe BiCMOS Tümleşik Devreler

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Özet

Onlarca yıldır, faz dizinli radar sistemleri, III-V yarı-iletken bazlı teknolojilerde üretilen alıcı/verici modülleri kullanmaktaydı. Fakat, bunların yüksek maliyeti, boyutu, ağırlığı ve düşük entegre edilebilme yetisi, alternative çözüm arayışları için bir talep oluşturdu. Son yıllarda, yüksek performans gereksinimlerini III-V teknolojilerine göre daha düşük maliyet ve güç tüketimiyle sağlamaları sayesinde, SiGe BiCMOS teknolojileri popülaritesini arttırtı. Yeni nesil faz dizinli radar sistemleri çok sayıda, tamamen tümleşik, yüksek verimli, küçük ölçekli ve yüksek kesinlikli alıcı/verici modüllerine gereksinim duyar. Bu eğilim doğrultusunda, bu tez, IHP 0.25µ SiGe BiCMOS teknolojisinde gerçeklenen, literatürdeki ilk ve tek X-Band 7-bit yüksek hassasiyetli faz/genlik kontrollü alıcı/verici modülünün tasarım ve uygulamasını sunmaktadır.

Bu tez kapsamında, düşük gürültülü yükseltici (LNA), SiGe HBT tek girişli çift çıkışlı (SPDT) anahtar, ve 7-bit dijital kontrollü adım zayıflatıcı gibi alıcı/verici devresi alt blokları kapsamlı bir şekilde tartışıldı. Tasarlanan LNA 1.7 dB gürültü sayısı (NF), 23 dB kazanç ve 16 dBm çıkışa endeksli 1-dB sıkışma gücü (OP_{1dB}) gösterirken; blok arası yükseltici ölçüm sonuçlarına göre 3 dB NF, 15 dB kazanç ve 18 dBm OP_{1dB} değerleri vermektedir. Buna ek olarak, tasarlanan SPDT 1.7 dB giriş kaybına (IL), 40 dB izolasyona ve 28 dBm OP_{1dB}'ye sahiptir. Son olarak, tasarlanan SiGe HBT 7-bit dijital kontrollü adım zayıflatıcı 8 dB IL, 0.18 dB etkin değer (RMS) zayıflatma hatası, 2° RMS faz hatası ve 16 dBm OP_{1dB} özellikleri göstermektedir.

7-Bit alıcı devresi yukarıda verilen blokların yanında 7-Bit faz kaydırıcı ve yüksek güç yükselticisi kullanarak yapılandırılmıştır. Serim sonrası simülasyon sonuçlarının gösterdiğine göre tasarlanan alıcı/verici modülü, X-Band frekansları boyunca, 38 dB kazanç, 2.6° RMS faz hatası, 0.82 dB RMS genlik hatası ve 80 dB alma-verme arası yalıtım göstermektedir. Alıcı verici devresinin yongası 11.37 mm^2 alan kaplamaktadır.

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List of Abbreviations

ANT	Antenna
APAR	Active Phased Array RADAR
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
CB	Common-Base
CE	Common-Emitter
EIRP	Equivalent Isotropic Radiated Power
FOM	Figure-of-Merit
Ge	Germanium
HBT	Heterojunction Bipolar Transistor
HB	High Breakdown-voltage
HP	High Performance
IF	Intermediate Frequency
I/Q	Inphase/Quadrature
iNMOS	Isolated NMOS
LNA	Low Noise Amplifier
LSB	Least Significant Bit
MEMS	MicroElectroMechanical System
NMOS	N-channel Metal Oxide Semiconductor
NF	Noise Figure
P_{1dB}	1-dB Compression Point
PA	Power Amplifier
PMOS	P-channel Metal Oxide Semiconductor
PS	Phase Shifter
RADAR	Radio Detecting And Ranging
RF	Radio Frequency
RMS	Root-Mean-Square
RX	Receiver
SiGe	Silicon-Germanium
SPDT	Single-Pole-Double-Throw
T/R	Transmit/Receive
TX	Transmitter
VGA	Variable Gain Amplifier
WWII	World War II
EM	Electromagnetic
SNR	Signal-to-Noise ratio

1. Introduction

1.1 A Brief Overview of Radar History

In recent years, Radio Detection and Ranging (radar) systems are used in countless applications such as satellite, military, collision avoidance, weather forecast, space observations etc. The radar is a system that determines distance, size, location, and velocity of a targeted object with a method based upon the reflection of radio waves.

Throughout the history, the first experiment for detecting an object with wireless signals was performed by Alexander Popov in 1897. In his experiment, he observed interference of a ship to a transmitted wireless signal [1]. The first radar, an anti-collision system operating at 650 MHz, *Telemobiloskop* was built by the German Christian Hülsmeyer in 1904 but his invention did not take attention of the market for approximately 30 years due to absence of any urgent need for radars and lack of efficient electronic devices as well as antennas to improve its performance [2]. During that period of time, even the crystal detectors was not practical and there was only spark gaps to create electromagnetic (EM) waves whereas the coherer was the only available detector, however, Hülsmeyer combined these components in a pragmatic way and became the patentee of the first radar which can detect ships within the range of 2 miles in dense fog [3].

Preparation period (1918-1944) for World War II (WWII) expedited research on radar systems and many countries including Italy, France, the Soviet Union, Germany, the United States, Japan, and the United Kingdom increased their investment on radar technology for military applications. These efforts are followed by the development of the initial mechanically steerable (physically positioning the antenna) radars during early 1930s. Due to the enhancements in electronics and performance limitations of mechanically steerable antennas, phased arrays in which main signal beam is steered electronically, are began to be employed in 1960s [4]. Today phased arrays are strongly preferable over mechanically steerable radars and being widely used in not only military but also civilian applications such as vehicle parking systems and smart houses.

1.2 Phased Array Radar Systems

Mechanically steered antennas provide a fixed beam-shape with low level and few number of side lobes. In addition, they operate in a wider frequency range at much lower cost with respect to phased arrays. However, they are deficient in scanning speed due to the need of physically positioning the antenna towards the desired direction. Moreover, some material failures and reliability problems may emerge, because continuous, inconsistent and fast movement of a heavy weighted antenna may cause fatigue on the servomotors. Furthermore, mechanically steerable antennas occupy a large space and consume much higher power than a phased array system that can perform equivalently. On the other hand, phased arrays are capable of exhibiting a high beam agility, low distribution loss as well as occupying much smaller area with high integration capability.

Performance requirements of an antenna system depend on the application they are being used. In the applications where information carrying signal is received from all directions or needs to be transmitted with an equivalent weight to everywhere, omnidirectional antenna systems are preferred. For example, omnidirectional communication has been used comprehensively in numerous applications because of its insensitivity to location and orientation of targeted objects, transmitters or receivers [5]. However, an omnidirectional antenna system suffers from several shortcomings such that a small fraction of transmitted power reaches to target because the transmitter radiates the electromagnetic (EM) signal in equivalent power to all directions. Therefore, for a given receiver sensitivity, a considerably high power has to be radiated by an omnidirectional transmitter [5].

On the other hand, in the applications where the signal needs to be transmitted towards a specific direction or received from intended source(s), directional antenna systems are required for a high antenna gain, high efficiency, high signal-to-noise ratio (SNR) and immunity to interfering signals. Systems utilizing high gain antennas possess narrow beams and low side lobe levels, hence, unlike the broad-beam antennas, a sharp, direction-based filtering of the transceiver antenna significantly attenuates the undesired out-of-beam signals [6]. For such applications, both mechanically or electronically steering antenna systems are convenient. However, in some

applications such as point-to-point wireless link, satellite and areal resource imaging, satellite communications, radio astronomy and automotive or military radars, phased array antenna based solutions are particularly suitable with their higher sensing range, higher SNR, functional versatility, rapid electronic beam steering, significant beamforming capability and high feasibility to digital programmability [7].

Phased array antenna systems have only been used for military applications in the past several decades because design of phased array radars involves and requires expertise on different areas such as antenna design, feeding networks, signal processing, beamforming/steering algorithms, prototyping and complex measurement which make phased arrays hard to implement and increase their cost [8] [9]. Complexity and high cost of phased arrays are primary hindrance to their utilization in large scale marketable applications, however, with the integration of fully monolithic Silicon-based process technologies into this area, there has also been a new growth in civilian based applications such as radar-based sensors, wireless local area networks, biomedical uses for cancer detection and advanced communication systems which have drawn an increasing interest in utilizing phased array technologies [9].

1.2.1 Operating Principles and Performance Metrics

As a general definition, antenna arrays are sets of radiators and receptors spaced at a specific distance apart from each other. When the individual antenna responses are added together, an array of antennas insert particular advantages over a single antenna system [10]. Antenna arrays can be composed of a few antenna elements to 4,000-10,000 antennas depending on the application. Figure 1 (a) represents architecture of a linear uniform antenna array consisting of N elements spaced with a distance of d apart from each other. As seen from the figure, if a signal comes from a targeted source, with an angle of θ to normal of the array aperture, the signal has to travel different distances to arrive each antenna on the array. The additional distance (∇d_{inc}) that an incoming signal must travel to reach the n-th element is given by:

$$\nabla d_{inc} = nd\sin(\theta) \tag{1}$$

As a result of the difference in distance that the incident wave must travel to reach each radiator, antenna elements receive the signal with a progressive time delay and phase difference.

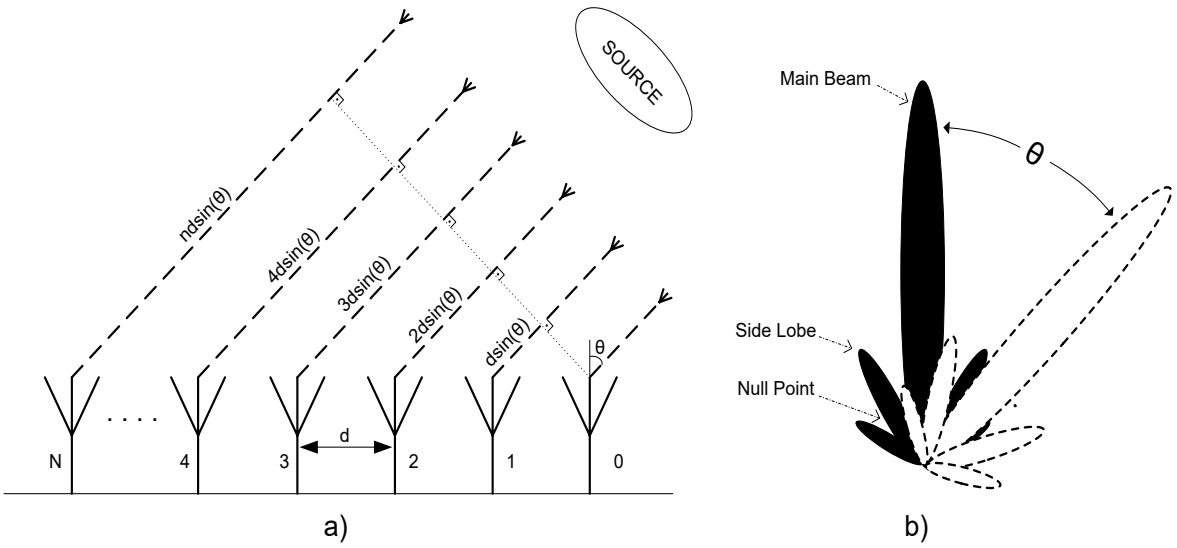

Figure 1: A uniform linear array with N elements

Equation (2) and (3) below represent the time (τ_n) and phase difference ($\emptyset_n$) for n-th element, respectively, where c is the speed of light, ω_c is the carrier angular frequency.

$$\tau_n = d\frac{\mathrm{n}\sin(\theta)}{c} \tag{2}$$

$$\phi_n = n\omega_c\tau = \omega_c d\frac{n\sin(\theta)}{c} \tag{3}$$

In general, the signal received by the first antenna element is given by the following equation where A(t) and φ(t) are respectively the amplitude and phase of the signal [5]:

$$S_0(\mathrm{t}) = \mathrm{A}(\mathrm{t})\cos[\omega_c t + \varphi(\mathrm{t})] \tag{4}$$

Similarly, the signal received by the *n*-th element can be expressed as the following equation [5]:

$$S_n(\mathrm{t}) = \mathrm{S}_0(\mathrm{t}-\mathrm{n}\tau) = \mathrm{A}(\mathrm{t}-\mathrm{n}\tau)\cos[\omega_\mathrm{c}\,\mathrm{t}-\mathrm{n}\,\omega_\mathrm{c}\tau+\varphi(\mathrm{t}-\mathrm{n}\tau)] \tag{5}$$

As seen from (5), the equal spacing among the antenna elements causes a progressive time delay τ and phase difference ω_ct in A(t) and φ(t).

Up to this point, time delay and phase difference issues for a receiver antenna array are explained, on the other hand, for the transmission mode, the same principles of operation are also valid due to the reciprocity of the system. If a progressive time delay is applied to adjacent antenna elements in an array, direction of the main beam in the radiation pattern can be deflected from its original position ($\emptyset$=0). Deflecting the direction of the main beam in the radiation pattern of an antenna array is called as *beam steering*. Figure 1 (b) represents a beam steering with the angle of θ in regard to normal of the array. The antenna arrays in which electronic steering of the main beam is provided by applying a time delay among the elements, are called as timed arrays. Additionally, the time delay between the adjacent elements can be compensated with a phase difference. Therefore, progressive phase shifting among the adjacent elements in an antenna array also provides deflection in the direction of the main beam. If the phase of incoming signal at each element of the array is selectively changed by using increments based on the spacing between adjacent radiators, the desired angle of transmitted or received radiation at which the array gain is maximum can be modified [10]. Such systems are called as phased arrays.

Timed arrays exhibit much wider operating frequency range with respect to phased arrays because progressive time difference between the adjacent antenna elements is independent to frequency of the incident signal. However, applying adjustable time delays between the elements is hard to implement while having performance limitations such as loss, noise and nonlinearity, especially across the RF frequency spectrum [5]. Consequently, recent radar applications demonstrate a growing interest in the antenna arrays utilizing phase shifters for electronic beam control. Phased array radars consist of thousands of antenna elements in which the phase and amplitude of the signal applied to each element can be controlled in such a way that creating an effective radiation pattern reinforced in the desired direction and suppressed in others [11]. As seen from Figure 1 (b), across the main beam, in both transmit and receive mode, the phase of wave fronts reaching to the each element or transmitted from them coincides with each other where a constructive interference occurs. In the direction of null points, phase of the received or transmitted signal collides with each other and a destructive interference takes place which attenuates (rejects) the signal.

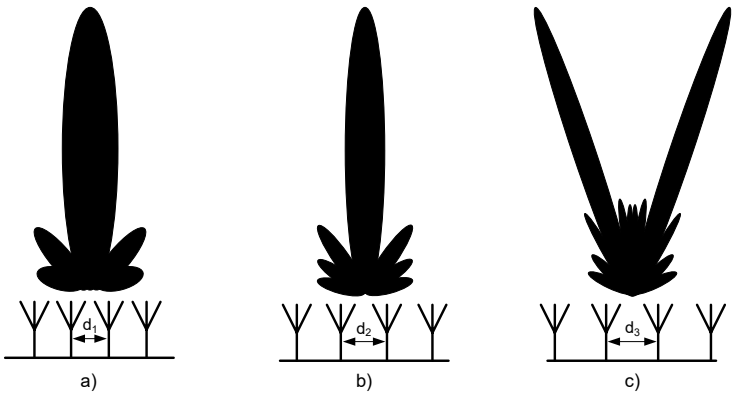

Figure 2: Radiation patterns of antenna arrays with an element spacing of a) $d_1 << \lambda/2$ b) $d_2 = \lambda/2$ and c) $d_3 >> \lambda/2$

As a result, in the receiving mode, incident wave coming from the direction of the main beam is coherently added with a relative power gain while out of beam signals are suppressed. By virtue of this characteristic, localization of the object becomes possible and more accurate because in an omnidirectional receiver there is no information given about the position of the object. Additionally, in radars utilized specifically in military applications, the rejection of interferer signals radiated by jamming devices is significant. Similarly, in the transmission mode, transmitted EM power is concentrated in the direction of main beam to increase the efficiency and sensitivity of radar.

The radiation pattern of an antenna array depends on the types of individual elements, their positions, orientations and the phase/amplitude of the signal feeding them. In order to simplify calculations for determining the radiation pattern of an antenna array, *element factor* (the pattern of each antenna) and *array factor* (the pattern of the whole array when all individual elements are assumed to be isotropic point sources) can be multiplied [12]. In other words, radiation pattern of an antenna array can be calculated by multiplying radiation pattern of a single antenna with array factor that is a function of array geometry and element excitations [13]. Normalized array factor of a long (L>>λ) and uniform linear antenna array is given by (6) where $\psi = \frac{2\pi}{\lambda} d \sin(\theta) + \phi$.

$$f(\psi) = \frac{\sin(N\psi / 2)}{N \sin(\psi / 2)} \tag{6}$$

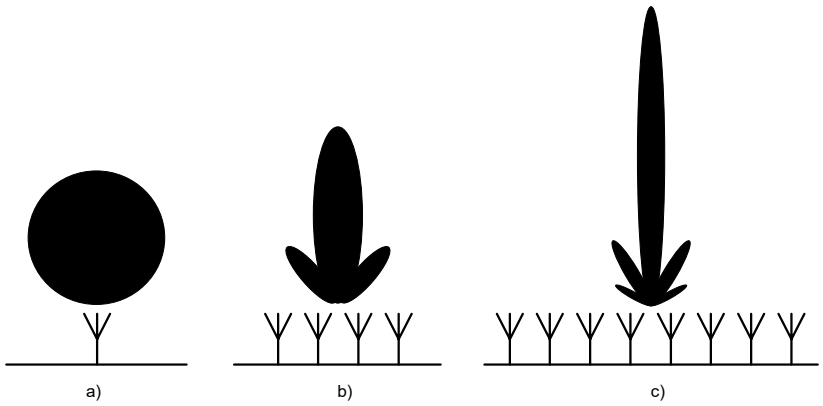

Figure 3: Radiation pattern of a) an isotropic antenna b) 4-element antenna array c) 8-element antenna array

As seen from (6), as number of elements increases, the main beam gets narrow and more side lobe levels appear in the one period of $f(\psi)$.

Additionally, spacing between the antenna elements also determines the width of the main beam as well as quantity, size and positions of the side lobes. Figure 2 represents variation in the width of the main beam with respect to changing distance between the antenna elements. As seen in Figure 2 (a) when spacing between the antenna elements is less than a one-half wavelength, main beam is not narrow while side lobe peaks are high. Furthermore, if the distance between the elements is set to a value above half-wave length (Figure 2 (c)) beam sharpness increases, however, as an important drawback there may be more than one major lobe called as *grating lobe* having intensity equal to that of main lobe. An extra main lobe can particularly be disastrous for the systems that utilized in military applications because signal coming from jamming devices may diminish the signal power of the target object. In order to prevent the formation of a second main beam, the spacing between the elements can be chosen to satisfy the following condition where θ_0 is the direction of maximum radiation:

$$\frac{d}{\lambda} < \frac{1}{1+|\cos\theta_0|} \tag{7}$$

Phased arrays generally use half-wave length element spacing (Figure 2(b)) to have acceptable main beam width and side lobe levels, simultaneously.

As seen in Figure 3 (a), radiation pattern of an isotropic antenna is spherical where as an antenna array consisting of 4 isotropic antennas (Figure 3 (b)) exhibits a more directive and higher gain radiation pattern due to the inherent advantage of array structure provided by wave interference phenomena. Furthermore, the 8-element antenna array shown in Figure 3 (c) demonstrates a narrower main beam width as well as higher gain and directivity with respect to 4-element array. Therefore, it is concluded that a greater number of elements in an antenna array increases directivity, gain and beam sharpness with the drawback of greater number (N-1) of side lobes. Directivity of a broadside ($L>>\lambda$) antenna array of isotropic elements can be approximated as the following [12].

$$D \approx 2\frac{Nd}{\lambda} \tag{8}$$

As seen from (8), higher number of elements and distance between the radiating elements, increases directivity of the array, as demonstrated in Figure 3.

In an N-element phased array system, total received signal power can be expressed as (9) where $S_{r,tot}$ is total signal power received by the array, $S_{r,ind}$ is power of incident signal received by each element and G_{ind} is power gain of each antenna [5]:

$$S_{r,tot} = N^2 G_{ind} S_{r,ind} \tag{9}$$

Since input signals of each element are added coherently, $S_{r,tot}$ is a factor of N^2 which means gain of an antenna array shows a square proportionality on number of elements included.

In the case when the antenna noise sources are uncorrelated, the output total noise power is given by [5]:

$$P_{N,out} = N(\mathrm{P_{N,ant}} + \mathrm{P_{N,}}_{rec})\mathrm{G_{ind}} \tag{10}$$

As seen from (9) and (10), signal power received or transmitted by the elements adds coherently whereas noise power adds incoherently, which results in a higher signal-to-noise and distortion (SINAD) in an array. Noise factor of an array is given by:

$$F = N \frac{SNR_{in}}{SNR_{out}} \tag{11}$$

For a given noise figure (NF), an antenna array consisting of N elements improves the receiver sensitivity by the factor of 10log (N). For example, N is 8, phased array improves the sensitivity by 9dB [5]. On the transmitter side, antenna array structure also increases effective isotropic radiated power (EIRP) by the factor of 20log (N) [14].

In addition, mutual coupling of the antenna elements must also be included into design considerations of a phased array because it can adversely affect feeding voltages and impedance values of the antennas. As a result, the level of the back radiation increases and the nulls of the radiation pattern becomes filled. Moreover, impedance matching gets worse and condition for maximum power transfer may not be satisfied. Consequently, efficiency of the array diminishes [15]. Therefore, spacing between the elements has to be adjusted by taking the mutual coupling into account.

Phased array radars has performance specifications based on quantity, single path (array element), and whole the antenna array. Quantity specifications cover operating frequency range, supply voltage and current consumption of the whole structure. Array element specifications are phase resolution, input return loss (RL), output RL, power gain, NF, isolation (output-to-input), RMS phase error, RMS amplitude error, group delay, input referred third-order intercept point (IIP_3) and area. General performance metrics of the whole array are RMS phase mismatch, RMS amplitude mismatch and isolation between the elements as well as array directivity factor and area. Moreover, maximum output power, sensitivity, EIRP, gain, 1-dB compression point, image signal attenuation, beam steering resolution, directivity etc. are some other performance specifications of phased array radars.

1.2.2 Phased Array Architectures

Phased array systems can be separated into groups based on the geometrical configurations of the antenna elements, the stage where phase shifting is applied to the signal and locations of Tx/Rx units.

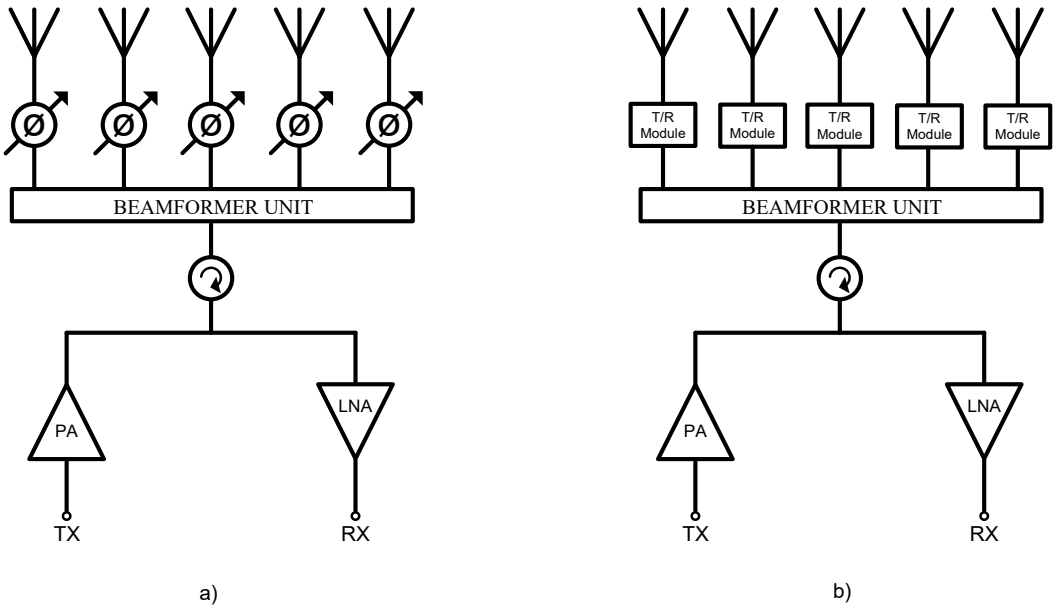

Figure 4: Circuit Diagrams of a) passive b) active phased arrays.

Depending on the placements of electronic T/R units, phased arrays can be assembled into two main groups such as passive phased arrays and active phased arrays. Figure 4 illustrates the circuit diagrams of passive and active phased arrays.

As seen from Figure 4 (a), in passive phased array structure, each antenna element has its own phase shift unit. On the receiver side, incident signal received by the elements are adjusted in phase and collected by beam former circuitry. Then, the received signal is directed to Rx node through a power limiter due to safety issues and an LNA for amplifying the signal to acceptable power levels. The main disadvantage of this topology is that the incoming signal firstly passes through a phase shifter which has high NF. Moreover, after the phase shifter, insertion losses (IL) of beam former, switch and power limiter also decrease SNR. Therefore, sensitivity of the receiver degrades. On the transmission side, the total power supplied by only a single power amplifier is also distributed among each antenna element. Consequently, power gain of each element is much lower compared to active phased array topology. In other words, detection range and gain of a passive phased array is lower than an active one. Additionally, if a malfunctioning occurs in PA, LNA, protector or switch, the whole array cannot operate anymore. Hence, passive phased arrays have also reliability issues. Advantages of utilizing a passive array is their low cost, high integration capability and the need of simpler data processors with respect to active phased arrays.

As seen in Figure 4 (b), in active phased arrays each antenna elements are self-contained their Transmit/Receive (T/R) module which will be discussed in subsequent section in detail. In the receiving mode, incident signal on an active phased array passes through LNAs which suppress NF being added by the following blocks. Therefore, NF and sensitivity of active phased arrays are superior to passive ones. In the transmission mode, active arrays are better than passive arrays in terms of gain and output power because in active arrays all the elements have their own PAs. Thus, detection and transmission range of active phased arrays are better than the passive ones. In addition, by virtue of T/R modules, the power weight of each element can be adjusted to decrease side lobe peaks and increase directivity by sharpening the main beam. Lastly, if one of the T/R modules suffers malfunctioning, an active phased array can still work properly which makes it highly reliable for military applications. As a disadvantage, active phased arrays require complex circuit structures, advanced computation algorithms, more design considerations and high cost. Passive phased arrays are initial topologies of phased arrays but advances in integrated circuit (IC) technology and data processing units enabled the utilization of active phased arrays.

There are also radio frequency (RF), intermediate frequency (IF), local oscillator (LO) and digital beam forming (DBF) architectures for phased arrays. In RF topology, phase shift is done in RF domain for all the elements whereas in IF structure phase is shifted in IF base. LO topology utilizes phase shift in LO path while DBF architectures performs digital phase shift. Each of these has particular advantages and disadvantages.

1.3 Transmit/Receive Module

In conventional active phased array radar systems, RF signal is distributed among each antenna element equipped by T/R modules in order to control phase and amplitude of the signal [16]. Modern Active Electronically Scanned Array (AESA) radar systems include thousands of T/R modules dominating the performance and cost of the radar system [17]. T/R modules consist of LNA, PA, phase shifter (PS) and single-pole double-throw (SPDT) switches for switching the signal between transmit and receive paths. In a T/R module there are two main sections or mode of operations, namely receive and transmit.

The receiver side of T/R module must be designed for optimum NF, IP_3 and IP_{1dB} performance because it determines the dynamic range of entire phased array radar. LNAs are essential blocks for amplifying the received signal with the addition of minimum possible noise as well as suppressing the noise added by the succeeding blocks. For a good noise performance at the receiver side, preceding blocks to LNA, such as SPDT switch, power limiter and antenna must exhibit minimum possible insertion loss (IL) because their losses directly contribute to the overall NF of the system. Power limiters are significant for limiting the power of incident wave to provide safety for the following blocks. After the LNA, there are phase shifter and amplitude control block for steering the main beam and adjusting the weights of antenna elements, respectively. As the last block, there is another T/R switch to route the signal to Rx node.

The transmitter side is usually designed for maximum power handling capability (P_{1dB}) for increasing the detection range of the AESA phased array radar system. The transmitted signal firstly passes through phase and amplitude control blocks for beam forming by selecting radiation angle of the radar and amount of radiation for each element. Then, the signal is applied as an input to the PA which is the main block that determines output power level. PA is generally the most DC power consuming block in a T/R module, thus, it effectively determines power consumption of the whole radar system. Lastly, transmitter side ends with a T/R switch to conduct the signal to the antenna. T/R switch must exhibit enough power handling capability to endure high power output signal of the PA.

1.3.1 T/R Module Architectures

Figure 5 represents several system level architectures for T/R modules. The topology shown in Figure 5 (a), has separate transmit and receive paths each including its own phase shifters and amplitude control unit (ACU). This architecture has a drawback in terms of area and cost because it employs dual PS and ACU. Moreover, it requires an extra control circuitry to adjust phase/amplitude of the signal due to additional PS and ACU. There are also alternative topologies (Figure 5 b) and c)) employing the same PS and ACU for both receive and transmit modes. Therefore, their area and cost efficiency are much higher with respect to a). However, a) has an advantage in IL because signal passes through only one SPDT.

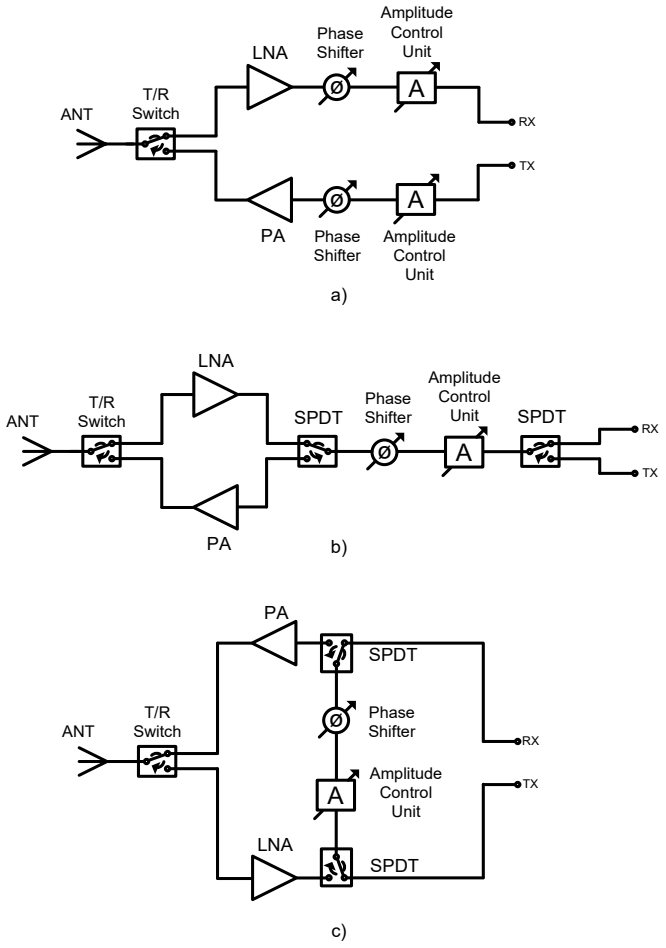

Figure 5: System level Circuit Diagrams for RF T/R Modules [18]

The T/R module architectures illustrated in b) and c) have almost the same performance parameters. In both of these, the signal passes through three SPDT switches across Tx-to-ANT and ANT-to-Rx paths, hence, ILs are the same. In b), isolation between Rx and Tx nodes are determined by the isolation of only one SPDT switch whereas in c) Rx and Tx are separated by two cascaded SPDTs across the receive and transmit paths. Consequently, c) exhibits better Tx-to-Rx isolation than b), which leads to decrease in possibility of cross-talk and instability in an AESA phased array radar. Lastly, in b) ACU must be capable of operating bi-directionally, nevertheless, in the topology c) there is no need for it. As a result, b) can only utilize attenuators as ACU while in c) Variable Gain Amplifiers (VGA) would have been employed. The use of VGA provides benefits of higher Tx-to-Rx isolation as well as higher gain at the cost of additional DC power consumption.

1.4 SiGe BiCMOS Technology

In RF/mm-Wave applications transistor performance is a bottleneck for achieving desired design characteristics. Some of the expected performance metrics of the transistors in high frequency applications are high current gain, high cut-off (f_T) and maximum oscillation frequency (f_{max}), low parasitic input resistance, small internal capacitances, high output conductance, low NF, reliability, radiation tolerance and decent power handling capability provided by high breakdown voltages. In the past, III-V technologies have been dominantly used for constructing T/R modules due to their high performance capabilities. However, as a consequence of ultimately high cost, low integration capability, lower yield, more difficult fabrication and higher power consumption of III-V devices, an alternative solution to design fully integrated T/R modules is required.

As an alternative to III-V technologies, RF CMOS technologies are also employed in some RF applications. However, RF performance characteristics of FET based devices are extremely layout-sensitive while high internal parasitic capacitances also degrade the RF properties. Although, FETs exhibit high f_T, f_{max} and low F_{min}, they strongly suffer from self-gain, impedance matching, 1/f noise and reliability under high signal powers [19].

By virtue of recent improvements in SiGe BiCMOS technology, T/R modules capabe to satisfy high performance requirements of phased array radars, can be built by employing SiGe technology. SiGe HBT BiCMOS technologies offer monolithic solutions for high frequency, performance constrained applications such as phased array radar systems, mm-wave communications and imaging systems [20]. As mentioned earlier, phased array radar systems include thousands of radiating elements which make area occupation critical for integration issues. Therefore, an affordable, highly integrated solution is desirable. This requirement makes SiGe HBT BiCMOS technology an appealing platform to implement a single-chip fully integrated T/R modules with on-chip digital control functionality [20]. Nowadays popularity of SiGe BiCMOS is increasing because common RF architectures are well suited to be implemented in combination of bipolar and CMOS devices [21]. Since the designed 7-Bit T/R module has digital control circuits, SiGe BiCMOS technology is selected to design and implement the system.

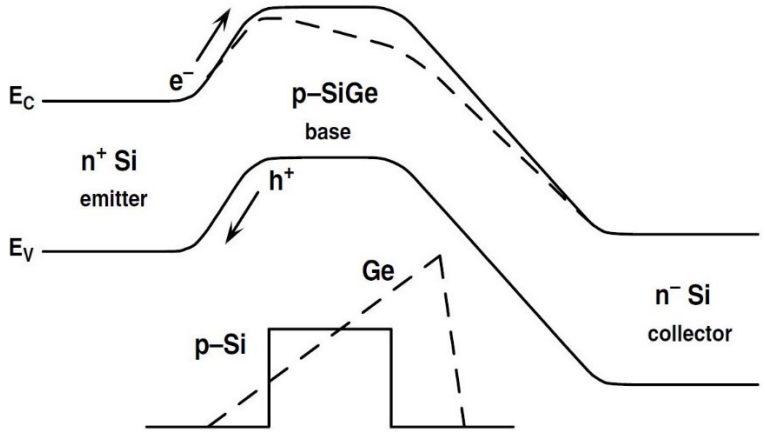

Figure 6: Energy Bandgap Diagram for SiGe HBT [22]

Introducing Ge into Si provides several advantages in performance characteristics of the devices. Figure 6 represents energy bandgap diagram of a SiGe HBT. In SiGe HBTs, the base is compositionally graded doped with Ge having bandgap energy is lower than Si. The position dependence in the Ge induced base region produces an additional electric field which leads to reduction in transition times (τ_b, τ_e, τ_c) between the nodes. SiGe HBTs bring the benefits of bandgap engineering to Si technology which contributes to increase in the current gain, early voltage and decrease in base transit time with respect to Si homo-junction NPN devices [19]. A Significant FoM in Bipolar transistors is the unity gain cutoff frequency, which is expressed as (12) where τ_b τ_e τ_c are the base, emitter and collector transition times respectively:

$$f_T = \left[\frac{1}{g_m}\left(C_{EB} + C_{CB}\right) + \tau_b + \tau_e + \tau_c \right]^{-1} \tag{12}$$

The increase in current gain puts a favorable impact on the f_T of the device [23]. In addition, as seen in (12), due to decreased transit time, f_T of the device increases, which translates to improvement in frequency response of the transistor. Moreover, for a given collector current density, SiGe HBTs require a lower V_{BE} with regard to Si BJTs, which translates to reduction in DC power dissipation. As an additional advantage of utilizing SiGe HBTs, achievable high current gain improves the input resistance and increases noise performance of the device [24]. As a consequence of all the advantages explained above, SiGe BiCMOS technology is employed for our 7-bit high phase/amplitude precision T/R module design.

1.5 Motivation

T/R modules are employed in variety of military and civilian applications. Especially in active phased arrays consisting of a few thousands of antennas, the performance, cost, size, weight, power consumption and efficiency of the overall system are determined by T/R modules. The previous generation T/R modules are realized by utilizing III-V semiconductor based technologies. However, due to their high cost, size, power dissipation and integration complexity alternative solutions are required. As a consequence of the recent developments in SiGe BiCMOS technology, now, it can offer HBT devices having performance parameters competitive to III-V technologies with much higher yield. In addition, since SiGe BiCMOS technology merged use of high performance bipolar transistors with CMOS devices on the same die. This opportunity enables realization of high frequency blocks and digital control units on the same chip, eagerly being utilized in modern RFIC applications.

The objective of this thesis is to design and implement an X-Band T/R module utilizing IHP 0.25um SiGe BiCMOS technology for phased array radar applications, which is the first 7-Bit T/R module in the open literature. The realization of a 7-Bit T/R module requires more complex design considerations with respect to the ones having lower resolution because the design must exhibit much lower RMS phase and amplitude errors. However, 7-bit PS and 7-Bit attenuator are successfully designed and inserted in the T/R module. For the realization of this project, the sub-blocks in the T/R module, such as LNA, SPDT switch, inter-stage amplifiers and attenuator are designed, implemented and explained in this thesis. As a novel contribution to previously designed T/R modules, the presented T/R module includes a 7-bit I/Q vector sum based phase shifter and a 7-bit digitally controlled SiGe HBT step attenuator which provide high resolution and high precision phase/amplitude control. Utilization of T/R modules having 7-bit phase/amplitude control capability provides particular advantages for the system level performance of phased array radars which will be comprehensively discussed in forthcoming sections.

1.6 Organization

This thesis includes five chapters which are organized as following:

Chapter 2 includes circuit design and analysis of the X-Band 7-Bit T/R module with high precision phase/amplitude control. Individual performance parameters of the sub-blocks are illustrated. Subsequently, significance and advantages of using 7-bit high precision phase/amplitude control T/R module in a phased array radar systems are discussed. The system level circuit configuration and specifications of the individual blocks are shown with summarized explanations. Afterwards, layout of the T/R module is demonstrated with the design considerations for compact and efficient chip design.

Chapter 3 begins with the design considerations for achieving low noise in LNAs and continues with how to obtain high linearity. Sections 3.4 and 3.5 consist of circuit analysis and measurement results of inductively degenerated 1-stage cascode LNAs utilizing IHP 0.13um and 0.25um SiGe BiCMOS technologies, respectively. In Section 3.6, design and measurement results of a 2-stage high dynamic range cascode LNA are demonstrated.

Chapter 4 explains design methodology of an X-band SiGe HBT SPDT switch to be used in our 7-bit T/R module. Moreover, performance parameters and their significances for the performance of the whole phased array radar system are discussed. Several novel methods to improve IL, power handling capability and isolation performance of the switch are introduced. Finally, comparison of the designed SPDT switch with similar work available in the open literature has been made.

Chapter 5 starts with the advantages of using attenuators instead of VGAs in T/R modules. Afterwards, it demonstrates design methodology and measurement results of a 7-bit CMOS Step Attenuator. Moreover, design and post-layout simulation results of an X-band 7-Bit SiGe HBT Digitally Controlled Step Attenuator is covered. As the final section, designed attenuators are compared with similar works in the open literature.

2. 7-Bit Fully Integrated T/R Module

2.1 Introduction

This chapter presents the design and implementation of an X-Band 7-Bit fully integrated single-chip T/R module with high precision phase/amplitude control. A SiGe BiCMOS process technology is employed due to its inherent advantages which are explained in section 1.4. The utilized IHP 0.25-μm SiGe BiCMOS technology offers three types of HBT and MOS devices. In this technology there are 3-types of HBTs namely high performance, mid-voltage and high voltage. RF parts of all blocks employ these transistors while digital parts including control blocks are implemented with MOS devices.

As mentioned before, the performance of active phased array radar is mainly determined by the performance of T/R modules. The designed 7-Bit T/R module includes a 7-Bit IQ based PS and 7-Bit digital step attenuator. The designed T/R module is the foremost in the open literature operating with 7-Bit resolution and it provides particular advantages for the phased array radar system. 7-Bit phase control provides advantages such that:

1. Capability of changing the phase with small increments enables directing the main beam in high resolution and detecting the location of an object more accurately.
2. Lower side lobe levels are provided by adjusting phases of individual radiating elements in such a way that except main beam direction, a destructive interference takes place. Therefore, more accurate phase adjustment leads to lower side lobe levels.
3. When the main beam is deflected via phase insertion to individual elements, in some directions radiation pattern cannot be focused due to requirement of fractional phase differences needs to be applied among adjacent elements. A 7-Bit T/R module can solve this problem and results in lower phase quantization error. For example, if 9° phase difference must be applied between adjacent elements, a 6-Bit PS with LSB of 5.6° causes at least 2.2° phase error while a 7-Bit PS can insert this 9° phase with the error of only 0.6°.
4. Phase shift with small increments can diminish random phase errors introduced by the other blocks in a T/R module such as attenuator. Consequently, phased array exhibits

lower phase error. Specifically in the radars where detection and ranging is based on the phase of the signal, lower phase error is highly desirable.

5. Lastly, in a phased array utilizing 7-Bit T/R modules, the same directivity can be achieved with smaller number of antenna elements with respect to the ones operating with less bit resolution.

In addition to 7-Bit phase control, the designed T/R module possesses high resolution amplitude adjustment capability with LSB of 0.25 dB by virtue of a 7-Bit digitally controlled step attenuator. In a phased array radar system, advantages provided by high precision amplitude control are given by:

1. At the null points, even the signal transmitted by the elements collide in phase and demonstrate destructive interference, if there is amplitude mismatch, the signal power cannot be completely diminished. However, with a high resolution amplitude control T/R module much better null points can be created.
2. In the same way, if there is an amplitude mismatch among the elements, side lobe levels and beam width increases while beam sharpness and directivity decreases. The designed T/R module minimizes amplitude mismatch between the antennas.
3. In this T/R module, amplitude error inserted by the PS and the other elements are compensated more effectively with respect to lower bit T/R modules. For example, if 0.3 dB amplitude error is inserted by the phase shifter, an attenuator with LSB of 0.5dB can reduce this error to 0.2dB while the designed 7-Bit attenuator can decrease this error to 0.05dB.
4. In a T/R module, amplitude variation across operating frequency band is also an undesired characteristic because complex amplitude calibrations require to be performed. The designed attenuator guarantees amplitude variation of at most 0.18 dB across X-Band and provides gain flatness.

In order to construct a 7-Bit T/R module, there exist many design challenges. 7-Bit effective bit resolution is only satisfied when RMS phase and amplitude error of the T/R module is less than half of the LSBs of the attenuator and phase shifter.

2.2 System Design and Analysis

Figure 7 illustrates system level circuit diagram of the designed 7-bit T/R module. This system configuration is selected due to compactness and reduced cost requirements. In this topology, the same PS and attenuator pair is utilized for both receive and transmit operations. By virtue of this, there is no need for placing separate PS and attenuator which translates to decrease in area and cost. Moreover, if seperate PS-Attenuator pair was used, there would be need for calibration to compensate any phase/amplitude mismatch among them, which means system complexity is also reduced owing to this circuit topology. In addition, this configuration provides good isolation between receive and transmit path. One of the most advantageous properties of this topology is the lack of requirement for bidirectional phase/amplitude control blocks allowing to use linear amplifier and an active phase shifter on the common part of receive and transmit paths.

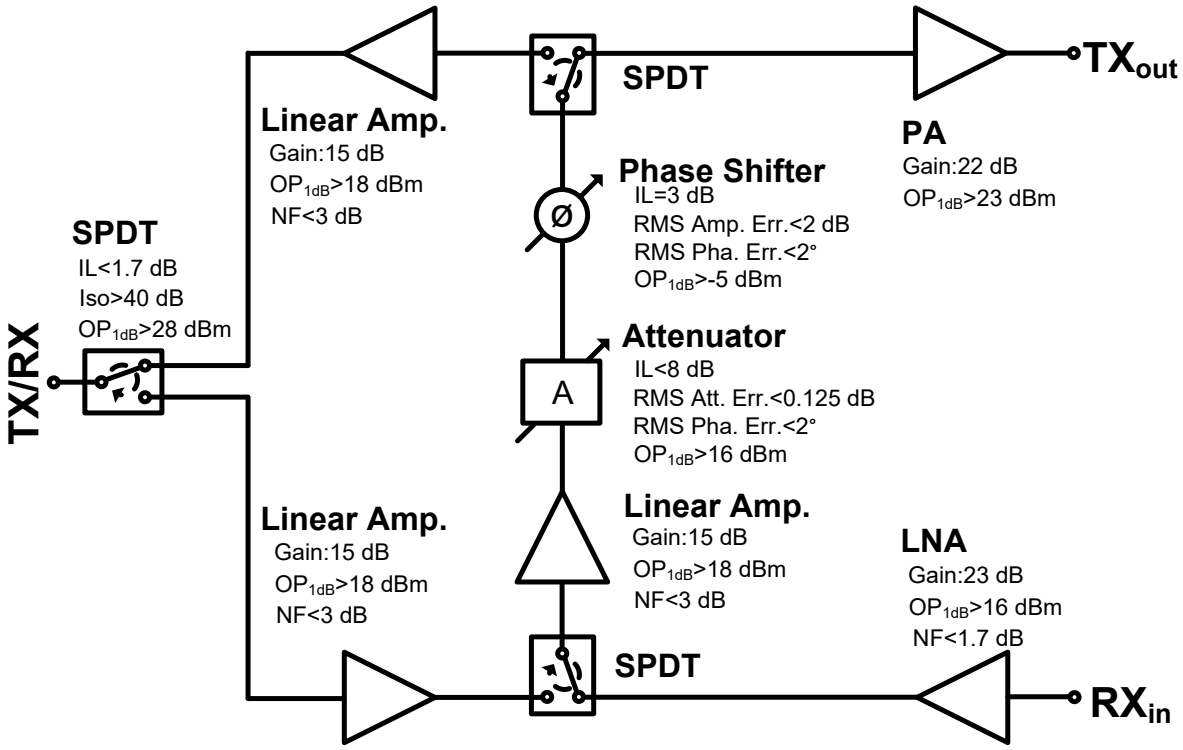

Figure 7: System level circuit diagram of the designed T/R Module with block level performances

As seen from Figure 7, the designed all-RF T/R module consists of an LNA, three SPDT switches, three linear inter-stage amplifiers, a PS, an attenuator and a PA. The detailed discussion about individual roles of the blocks for the system level performance are made section 1.3. Performance parameters of the utilized blocks are also shown in Figure 7. In contrast to conventional T/R module structure, linear inter-stage amplifiers are placed in this project with the aim of achieving enough gain and compensating ILs of PS, attenuator and SPDT switches. In addition, inter-stage amplifiers also decrease NF of the system because they are designed for low NF and high gain.

2.3 Layout Construction

IHP 0.25-µm SiGe BiCMOS technology is employed for the realization of this T/R module. Figure 9 represents the designed layout of the T/R module. Since, the occupied area of the T/R module is critical for the cost and size of a phased array, this layout is planned for minimum area occupation. The constructed T/R module die occupies an area of 11.37 mm^2 which is much smaller than the similar work employing III-V semiconductor based technologies.

This T/R module is not designed as a whole system. Firstly, expected performances from each block is determined by using Advanced Design System (ADS) tool. Afterwards, the blocks are designed, implemented and measured separately. Then, they are combined and the 7-bit T/R module is constructed.

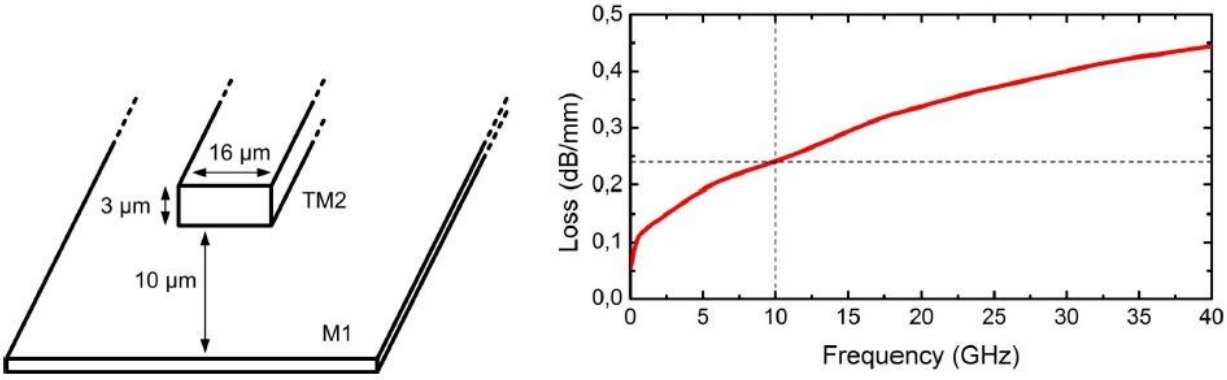

Figure 8: The utilized 50Ω transmission line for interconnections and simulated IL of it [18]

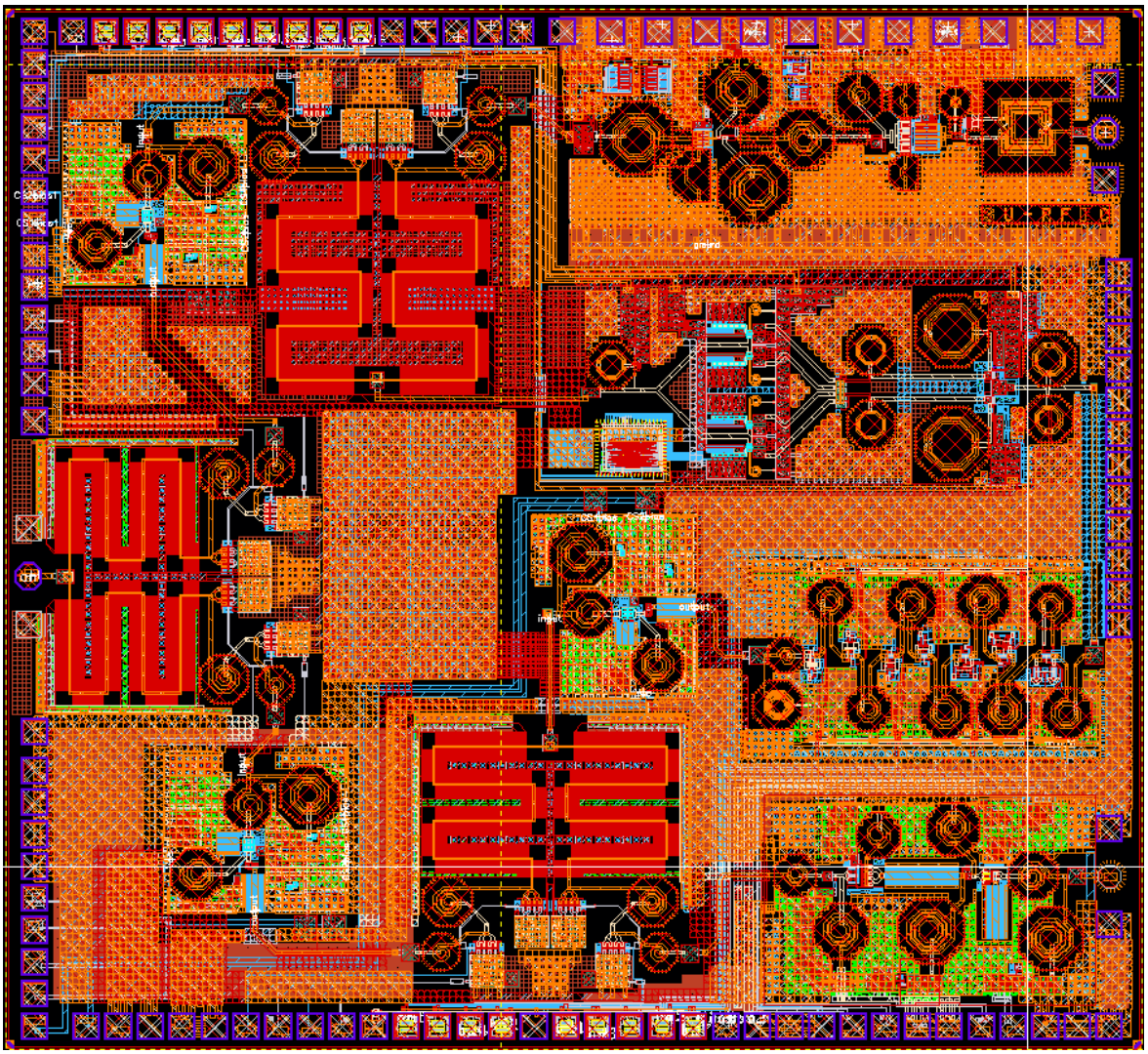

Figure 9: Layout of the designed 7-Bit T/R module

In order to prevent degradation in the performance of the whole system due to long inter-connections between the adjacent blocks, they must be placed close to each other. Moreover, a proper transmission line has to be designed for minimum IL. Due to design each sub-block separately, combining them in a compact configuration requires long interconnections. Figure 8 represents dimensions of the utilized 50Ω transmission line for connecting the individual blocks in the designed T/R module.

3. X-Band SiGe HBT Low Noise Amplifiers

3.1 Introduction

In T/R modules, an LNA is the first amplification block at the front end of receiving path placed right after the T/R switch. As a result of being the first block on the receiver side, main responsibility of an LNA is to provide sufficient gain to overcome the IL and NF of proceeding blocks such as SPDT switch, PS and attenuator, while exhibiting a low NF because the individual NF of LNA sets a lower bound for the NF of the whole receiver [25]. In a radar structure, LNA is one of the most critical components to determine receiver sensitivity (e) of the whole system [26].

$$e = \sqrt{(F_{OC} + F_{IM} + F_{LO})kTB(R\text{-}1)R_Z} \quad \text{(V)} \tag{13}$$

Receiver sensitivity of a radar is formulated in equation (13) where F_{OC} is noise from on-channel, F_{IM} is the noise caused by image frequency and F_{LO} is the wide-band noise generated by local oscillator while k is Boltzmann's constant, T is temperature (K), B is bandwidth, R is (S+N)/N at detector input and R_Z is system impedance. In a radar system, F_{IM} and F_{LO} can be reduced by the insertion of filters, however, the F_{OC} which propagates throughout the RF front-end in a cascaded topology is predominantly set by the LNA [26].

One of the key challenges of many radar applications is their ability to receive incident signal over a wide range of input powers [27]. The next generation phased-array radar systems target T/R modules exhibiting high performance in terms of dynamic range [28].An improved dynamic range in the receiver would benefit a number of system-level performance metrics such as lower required transmit power, increase in minimum detectable signal (MDS) and increase in immunity to interfering signals [27]. LNA is the crucial component to satisfy stringent requirement for high dynamic range (HDR) in a T/R module since they strongly contribute to system NF as well as 1-dB compression point (P_{1dB}) and system intermodulation distortion measured by third-order intercept (IP_3) [27] [28].

In applications where large arrays with high number of antenna elements are used, the DC power dissipation of the LNA turns into a significant factor as the receivers generally needs to be

continuously powered [29]. However, there is a trade-off between NF, gain and linearity performances of an LNA. The compensation of trade-offs depends on applications in which ultra-low NF may not be a priority due to the need of lower power consumption to provide longer battery life-time of portable communication systems [30]. Moreover, some applications such as high-altitude and space-based low power density phased array radar systems require a receiver with ultra-low power dissipation due to limited power supply of the radar platform [31]. In addition to NF, gain and power handling capability, input return loss (RL) and output RL are also two important specifications for LNAs because a good impedance matching with preceding and following components provides unconditional stability and more efficient power transfer between the sub-blocks.

In the past, LNAs are preferred to be designed by using III-V technologies instead of Si-based fabrication processes. Nonetheless, by the emergence of SiGe HBT technology employing bandgap engineering in order to improve transistor performance, all these high performance requirements can be achieved while sustaining strict compatibility with conventional Si CMOS manufacturing. SiGe HBT technology combined decent performance of III-V transistors with the high integration levels, low cost and high yield of conventional Si-based technologies to facilitate realization of fully monolithic T/R modules [32].

3.2 LNA Design Methodology

As an initial step to design an LNA, circuit topology must be selected by taking the specifications and trade-offs into account. There are three main configurations for amplifier design which are common-collector (CC), common-base (CB) and common-emitter (CE). CC topology exhibits high input and low output impedances, thus, they are suitable candidates to be used as buffer [30]. CB amplifiers provides high gain and good linearity but has narrow band operation due to low (1/gm) input impedance. CE emitter configuration performs well in terms of gain and NF but has a drawback of increased miller effect which diminishes reverse isolation and stability of the amplifier. The most frequently employed LNA structure is utilization of CB as a cascode in combination with a CE driver stage [30]. This circuit topology is known as cascode topology which provides particular advantages such as higher gain, increased reverse isolation, broadened

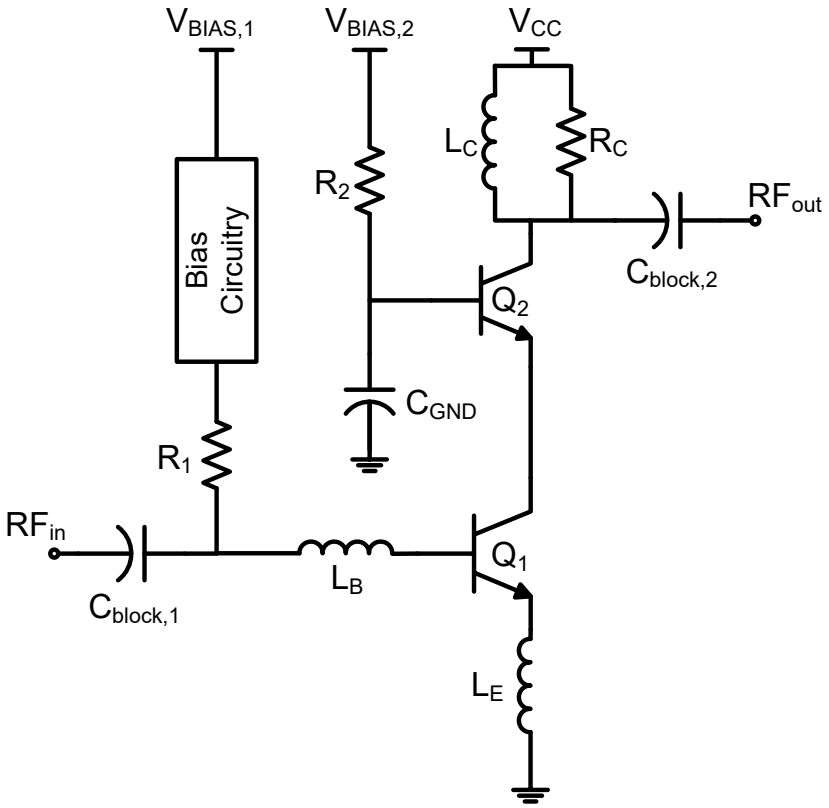

Figure 10: Schematic view of a conventional cascode LNA

operating frequency range and more reliable stability issues over conventional CE amplifiers with the cost of slightly higher NF and DC power dissipation.

Figure 10 represents schematic view of a conventional cascode LNA. As shown in Figure 10, the input transistor Q_1 operates as a transconductor and provides the gain of the amplifier whereas CB transistor Q_2 acts as a unity gain buffer and improves the gain performance by enhancing reverse isolation and reducing the effect of miller capacitance of Q_1 [33]. Moreover, $C_{block,1}$ and $C_{block,2}$ block DC current flow to RF_{in} and RF_{out} nodes while adjusting input and output impedance matchings as well as frequency of the gain peak. C_{GND} grounds the base of Q_2 for AC signal in order to obtain CB operation from this stage. R_1 and R_2 prevent AC signal leakage towards the bias points. Therefore, R_1 and R_2 resistors have to be selected high to avoid power loss and additional NF at the input side (R_1). The inductor L_C serves for loading the output and biasing the collector of Q_2 as well as adjusting the frequency where the gain has its peak value.

After the selection of circuit topology to design LNA, transistor must be selected among those available in the technology. The IHP SiGe BiCMOS technology employed to realize LNAs, have 3 types of HBTs including a high performance, medium voltage and high voltage in the library. If the main design concern of the LNA is to achieve high power handling capability, medium voltage or high voltage HBTs can be utilized. However, in this case, NF of the LNA increases due to their low f_T/f_{max} values. Minimum NF for an inductively degenerated cascode LNA is given by (14) where β is current gain, *gm* is transconductance, f is operating frequency and f_T is unity gain cut-off frequency of the utilized transistor [31].

$$NF_{\min} = 1 + \frac{1}{\beta} + \sqrt{2gmr_b}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T}\right)} \tag{14}$$

As seen from (14), if the primary specification of the LNA is to obtain optimum NF, the transistor with the highest f_T has to be selected because as f_T increases minimum achievable NF decreases while the linearity of the LNA declines due to smaller voltage swing range caused by lower breakdown limit of the transistor.

In HBTs, when the collector current is low, thermal noise is dominant while in the case when the collector current is high, shot noise becomes the main noise source. For that reason, there is an optimum collector current where the transistor exhibits minimum NF. The following step in LNA design methodology is to determine optimum collector current density ($J_{C,\,OPT}$) for minimum NF while using equally sized Q_1 and Q_2 transistors as unit cell because $J_{C,\,OPT}$ of single transistor Q_1 is different from $J_{C,\,OPT}$ of cascode topology [11]. $J_{C,\,OPT}$ can simply be determined by scaling bias voltage of the unit cell costing of cascode connected Q_1 and Q_2. The collector current density on which NF takes the minimum value is called as $J_{C,\,OPT}$.

The next step is selecting number of devices in order to adjust emitter length of the devices. If noise impedance is matched to system impedance (typically 50Ω), simultaneous noise and power match can be obtained.

$$R_{S,OPT} = \frac{f_T}{f}\frac{1}{\ell_E}\sqrt{\frac{2}{J_C}\frac{r_b \ell_E}{W_E}\frac{kT}{q}} \tag{15}$$

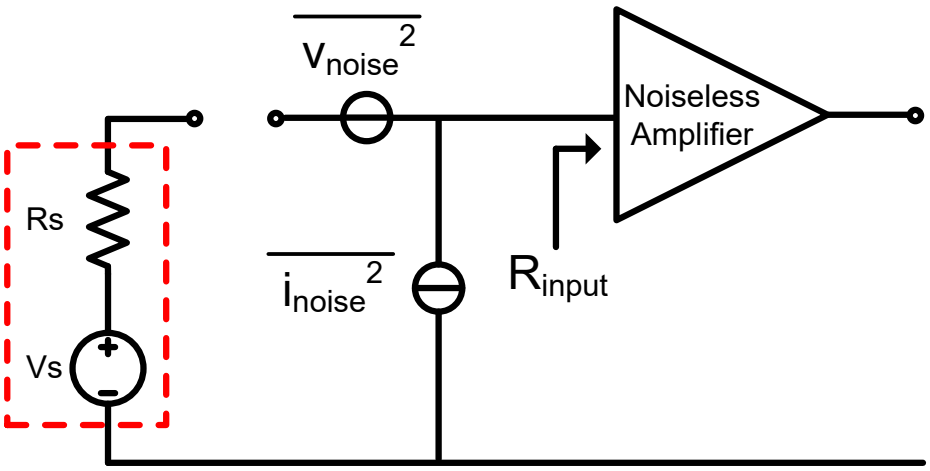

Figure 11: Illustration of power and noise matching in an amplifier

Optimum source resistance that Q_1 must be terminated to have minimum NF is shown in equation (15) where ℓ_E and W_E are emitter length and width, respectively.

It is seen in the equation that $R_{S,\,OPT}$ can be adjusted to the system impedance by scaling emitter length, ℓ_E of Q_1. Adjusting the emitter length to make $R_{S,\,OPT}$ equal to 50Ω is significant because this adjustment eliminates the need of lossy matching elements for noise matching.

After the noise matching has been completed, power matching is the next step to perform. Figure 11 represents illustration of matching a voltage source and an amplifier for minimum NF and maximum power transfer.

If v_{noise} and i_{noise} are assumed to be uncorrelated, noise matching is completed when $R_S = \sqrt{v_{noise}^2 / i_{noise}^2}$ while the power matching condition is satisfied when R_S is equal to R_{input} [34]. Simultaneous power and noise matching can be performed by adjusting base inductor L_B and emitter inductor L_E where ℓ_E has already been predetermined. In cascode topology, input impedance can be approximated as input impedance calculation of a CE amplifier by ignoring the CB stage. First of all, derivation of input impedance of a CE HBT amplifier that is not inductively degenerated (no L_E and L_B), can be expressed as (16).

$$Z_{Q1} \approx r_b + r_e + r_\pi \left(\frac{\omega_T}{\omega \beta_0} \right) - j \left(\frac{1}{\omega C_\pi} \right) \tag{16}$$

The input impedance without L_E can be expressed as equation (16) where β_0 is low frequency ac current gain, r_b and r_e are base and emitter parasitic resistances while r_π and C_π are, respectively, base-to-emitter parasitic resistance and capacitance. Since ($r_b + r_e$) is optimized for minimum NF and has very small values as well as r_π, (16) shows that input impedance without L_E and L_B rapidly decreases with increasing frequency [35].

On the other hand, if L_E and L_B are included in the amplifier topology when parasitic resistances are neglected, Z_{Q1} equation transforms into following [36].

$$Z_{Q1} \approx gm_1 \frac{L_E}{C_\pi} + j\left[\omega(L_E + L_B) - \frac{1}{\omega C_\pi}\right] \tag{17}$$

Equation (17) shows that, since Cπ is constant due to predetermining ℓ_E in the previous stage, real part of the input impedance can be set to 50Ω by scaling only L_E. In addition, the imaginary part of the input impedance can also be cancelled by adjusting base inductor L_B.

As the last step, output impedance matching must be performed by adjusting values of L_C, R_C, $C_{block,2}$ and emitter length of Q_2 ($\ell_{E,2}$). After the final optimizations are made, schematic design of an LNA is completed. Layout has to be done as small as possible while taking parasitic effects such as the inductive effects of bond wires and capacitances of DC pads into account.

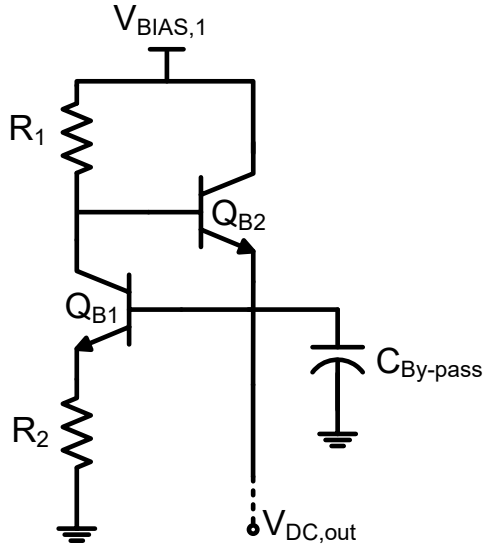

Figure 12: The schematic view of utilized active bias circuitry

3.3 Active Bias Circuitry

As mentioned before, in LNAs, linearity and P_{1dB} performances are key specifications for overall system performance. Applying more collector current may increase the power handling capability of the LNA, however, NF also increases. In addition to higher collector current, utilizing active bias circuitry for biasing the base of the device Q_1, also increases saturation power level of the LNA. Therefore, in all the LNAs that will be presented in the remaining part of this chapter, active bias circuits are employed which is shown in Figure 12.

When a large signal is received by an LNA, base-to-emitter voltage (V_{BE}) fluctuates due to changes in the base current of Q_1. This fluctuation causes drop in saturation power level and degradation in the linearity of LNA. Active bias circuitry prevents voltage to vary with the applied RF signal and contributes to increase in power handling capability of the LNA. Especially in the case where an inductor (L_{BIAS}) is placed instead of R_1, $V_{DC,out}$ becomes even less dependent on the base current variations. Therefore, in all the designed LNA structures, an inductor L_{BIAS} is employed as RF-choke for achieving higher linearity. In addition, employing an inductor as RF_{choke} increases IIP_3 performance as low frequency harmonics are grounded through $C_{By\text{-}pass}$. Consequently, risk of low frequency oscillation is eliminated whilst stability and dynamic range of the LNA also increases at the cost of slight increase in NF and narrow band input RL.

3.4 An X-Band High Dynamic Range Flat Gain LNA

This section presents the design and implementation of a single-stage hetero-junction bipolar transistor (HBT) LNA operating in X-Band. The LNA is implemented in IHP 0.13-µm SiGe BiCMOS process technology. In this technology two types of HBTs are offered namely high performance and high voltage devices. There are two options for high performance HBTs with cut-off frequencies (f_T) of 250 GHz and 240 GHz while having almost similar C-E breakdown voltages (1.7 V). On the other hand, high voltage transistor has a relatively low f_T of 40 GHz, nonetheless, provides much better power handling capability with respect to high performance devices.

The primarily aimed performance parameters for this LNA are to obtain high power handling capability and flat gain without compromising NF performance and power dissipation.

Therefore, an inductively degenerated cascode topology with RC feedback mechanism is used in order to obtain low NF, high stability (reverse isolation), high linearity and high gain with low variation across X-Band. In addition, HBTs are biased for the objective of achieving maximum possible power handling capability and acceptable NF performance.

3.4.1 Circuit Analysis

Figure 13 represents schematic view of the LNA. As seen in the figure, active bias circuits are employed to bias base nodes of the high performance devices Q_1 and Q_2 in order to obtain high power handling capability despite their limited breakdown voltages. In this LNA design, high voltage devices are not employed because as previously mentioned, lower f_T causes high NF. The methodology that is followed while designing this LNA is a bit different from a conventional cascode topology due to use of R-C feedback. In this LNA configuration, input impedance is not only a function L_E, L_B and emitter length of Q_1 because R-C feedback mechanism creates interdependence between output and input impedance matching networks where L_1 is also affective on input matching in contrary to conventional LNA structure.

The primarily aimed specifications for this LNA are high P_{1dB} and at least 15 dB gain centered along 10 GHz with low variation across X-band (8-12 GHz) frequencies while the NF is also lower than 1.5dB. RC feedback circuitry consisting of R_1 in series with C_1 is added for adjusting the flatness and center frequency of the gain of the LNA. However, the gain and reverse isolation decrease due to additional path from output to input while NF gets higher owing to extra noise source R_1 and output matching network. Moreover, as a result of previously highlighted trade-off between high gain and NF performance, the designed LNA exhibits a little higher NF because collector current densities of the HBTs are needed to be higher than $J_{C,\,OPT}$ to compensate reduction in the gain dictated by RC feedback technique. Sizes of Q_1 and Q_2 HBTs are adjusted for the purpose of providing sufficient collector current to prevent saturation in output signal power.

In addition, the RC feedback circuit basically creates a resistive path from output port to input port of the LNA and also contributes to wideband S_{11} and S_{22} values by reducing quality factor of the matching networks.

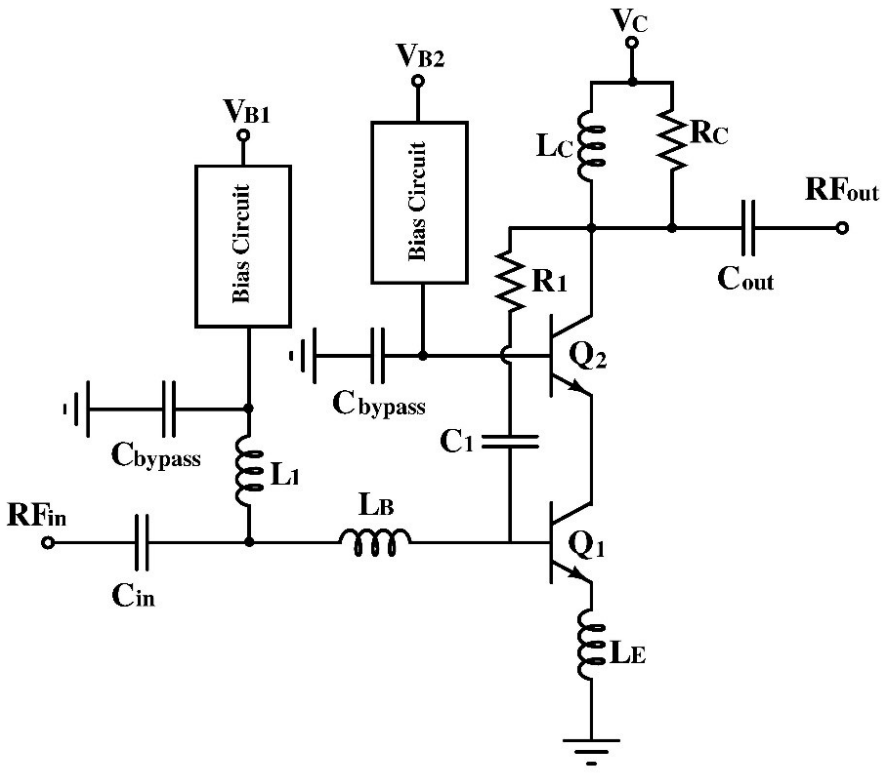

Figure 13: Schematic of X-band high dynamic range flat gain LNA

In order to obtain high linearity, base-emitter bias voltage of the device Q_1 is applied through an inductor L_1. Instead of a resistor, an inductor is used as RF-choke because voltage drop on the resistor significantly changes with the variation in power of RF input signal. As a consequence, resistors cause reduction in linearity of the LNA. The inductor L_1 also shunts low frequency harmonics of the input signal which translates to prevention of low frequency oscillation and stronger immunity to interfering signals.

Moreover, base voltage of the device Q_2 is also critical for power handling capability since it determines voltage drop on the collector of Q_1. The collector-to-emitter voltage of Q_1 is adjusted near breakdown voltage to provide maximum voltage swing for output signal of the CE stage. The collector voltage of the device Q_2 is also applied as sum of collector-to-emitter breakdown voltages of each HBT for the purpose of having maximum voltage swing at the output in order to achieve desired output signal power.

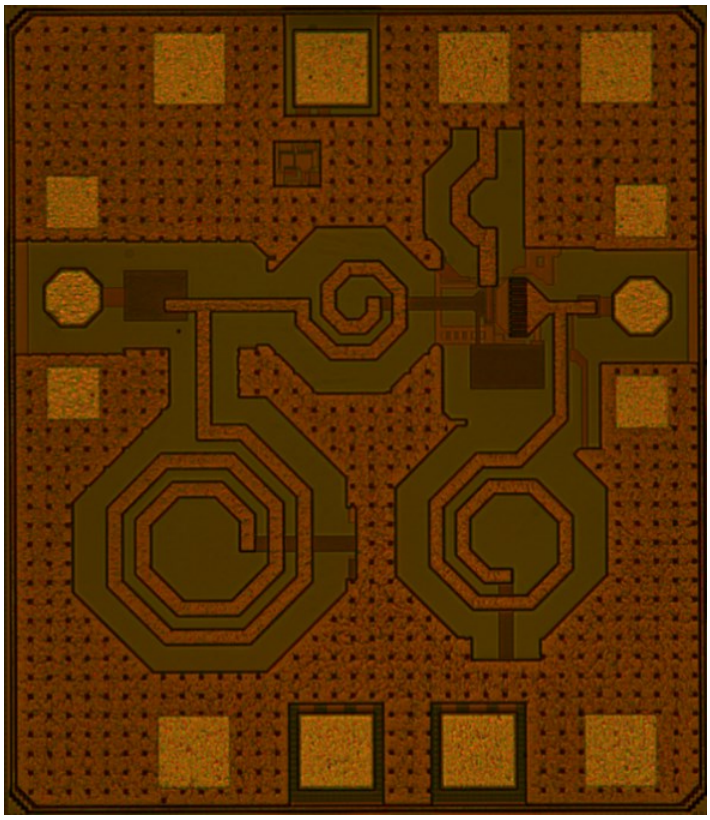

Figure 14: Die view of the X-band HDR flat gain LNA

3.4.2 Measurement Results

The designed LNA is fabricated in IHP 0.13-µm SiGe BiCMOS process technology. Figure 14 represents snapshot of the measured X-band HDR flat gain LNA die which occupies an area of 0.61 (0.73 x 0.84) mm^2. Q-factors of the L_E, L_B and L_1 inductors are critical for NF performance because internal parasitic resistances directly increases NF due to being at the front-end side. For this reason, they are custom designed in octagonal shape by employing the highest and most conductive metal layer in order to obtain higher Q-factor and less substrate coupling. Moreover, for the aim of modelling the layout properly, all inductor and interconnections among the components are simulated via SONNET. The chip is biased as per values determined during the schematic design and the same DC characteristics are also measured. The chip dissipates 23.1 mW of DC power. Measurement of the LNA is performed as following the methods demonstrated in Appendix A.

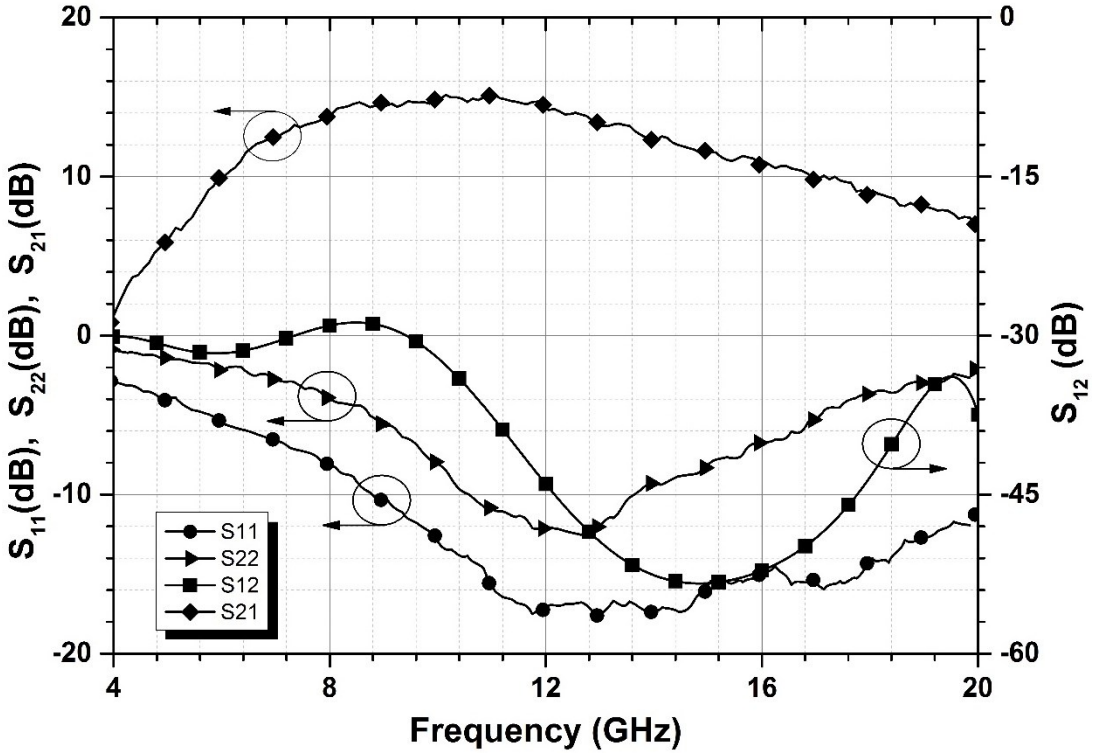

Figure 15: Measured S-Parameters of the LNA

Figure 15 shows the measured S-parameters of the LNA. As seen from the graph, the LNA exhibits a high and wideband reverse isolation (S_{12}) of more than 29dB which means that the LNA has no risk of oscillation near the frequency band of interest. In addition, it provides a wideband input RL of more than 8dB with an acceptable output RL across X-Band. The gain of the LNA is 15dB at 10 GHz with the variation of $\pm$0.5dB across X-band frequencies which is a state-of-art gain flatness performance.

Figure 16 represents measured and simulated NF of the LNA. The measured NF is less than 3.2 dB in X-band with a minimum value of 2.6 dB at 9 GHz whereas simulated NF is less than 2dB in a wide frequency range. The main design concern was not to achieve minimum NF. A high linearity was the primary goal of this LNA and it is obtained at the cost of an increase in NF. Figure 17 illustrates the measured P_{1dB} of the LNA which has an input referred value of 3.6dBm and an output referred value of 17.6 dBm. Despite the limited breakdown voltages of HBTs in utilized technology, achieving 17.6 dBm OP_{1dB} is a consequence of proper biasing of HBT devices and accurate RF modelling of the design.

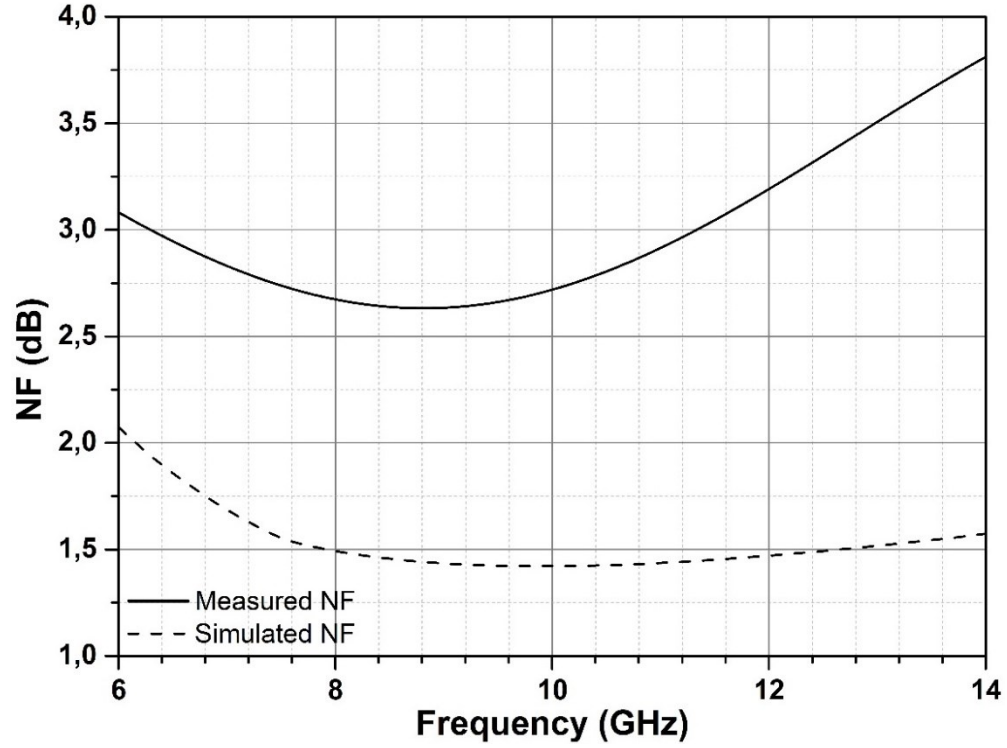

Figure 16: Measured NF of the LNA

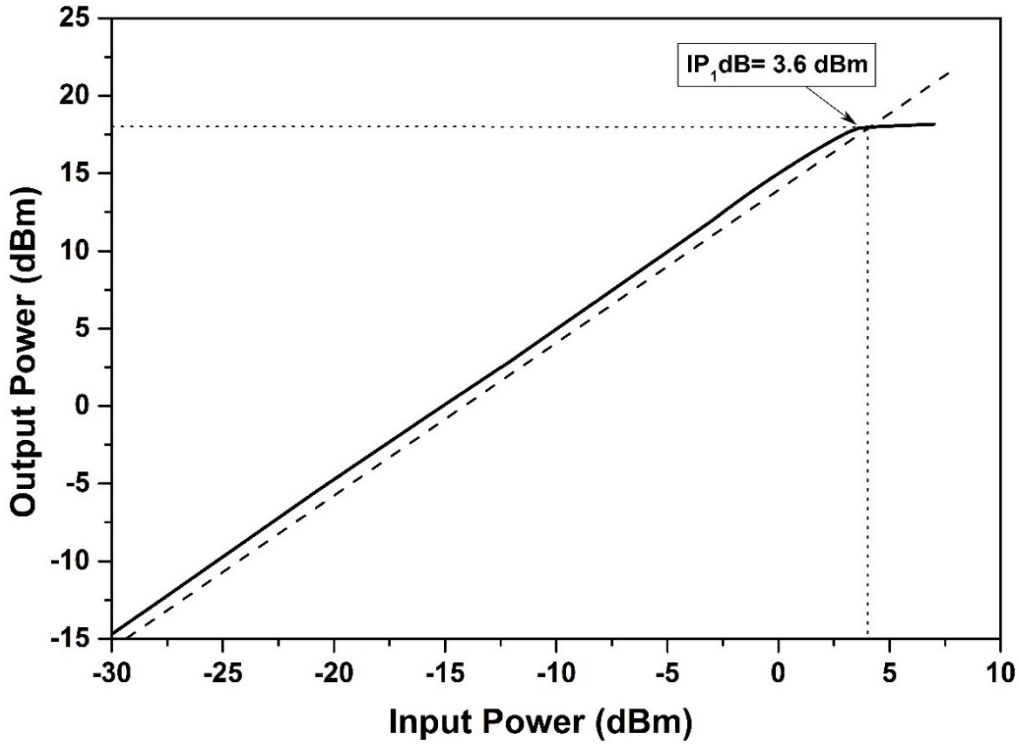

Figure 17: Measured 1 dB Compression Point of the LNA

Table I: Performance Comparison with the other 0.13-µm SiGe HBT LNAs in the Open Literature

Reference	**This work**	[37]	[31]	[27]	[32]
Frequency	10GHz	10GHz	10GHz	9.5GHz	9.5GHz
Noise Figure	2.7dB	1.36dB (mean)	1.98dB	2dB	2.78dB
Gain	15 dB	19.5dB	10dB	30dB	11dB
Input-P1dB	3.6 dBm	-10dBm	-10dBm	-11.5dBm	-19.1dBm
Power Consumption	23.1 mW	15mW	2mW	285mW	2,5mW
Die Area	0.61mm^2	0.526mm^2	0.436mm^2	1.76 mm^2	0,52 mm^2
Figure-of-Merit	**21.2**	5.46	3.99	1.87	0.39

3.4.3 Benchmarking

Table I represents performance comparison of the LNAs available in the open literature, which are implemented in 0.13-µm SiGe BiCMOS technology. In comparison to the other X-band LNAs in the open literature, this LNA is better than previously reported ones in terms of input matching, 1dB compression point and gain while dissipating low DC power. The figure-of-merit given below is used for benchmarking the LNAs in the open literature.

$$FoM_{LNA} = \frac{G[abs.]IP1[mW]}{P_{\text{supply}}[mW]} \frac{1}{(NF-1)[abs.]} f[GHz] \tag{18}$$

As seen in the table, the designed LNA has much better FoM with respect to similar work available in the open literature. Its high power handling capability and low DC power consumption are main factors that contribute to achieve higher grade calculated by (18). In spite of relatively high NF of the measured LNA, it is better than other LNAs when the overall performance is evaluated by taking all the specifications into consideration.

One of the most significant performance characteristics of the designed LNA for the system performance is its flatness in the gain which is not included in the utilized FoM equation. Flat gain is an important specification and advantage because phased array radars need to be calibrated if gains of T/R modules are varying in the frequency band. At the receiving end, utilization of a flat gain LNA decreases need of calibration and facilitates operation of the whole RADAR system.

3.5 An X-Band High 1-dB Compression Point SiGe HBT LNA

In phased array radar applications thousands of highly linear, high gain, efficient and low noise T/R modules are utilized. Due to the need of highly linear T/R modules, LNAs must be able to operate when the power of incident wave is very high, in order to prevent saturation in the system gain and provide immunity to 3rd order harmonics. Therefore, an X-Band high P_{1dB} LNA is designed and implemented to be placed in the front end of T/R switch.

This section presents the design scheme and implementation of an X-Band LNA with high linearity. The LNA exhibits very high linearity with relatively low DC power consumption, nevertheless, NF performance is not enough to employ this LNA as the first block at receiving side. Therefore, it is used as inter-stage amplifier with the intention of suppressing NF of the PS and compensate for the IL of the attenuator.

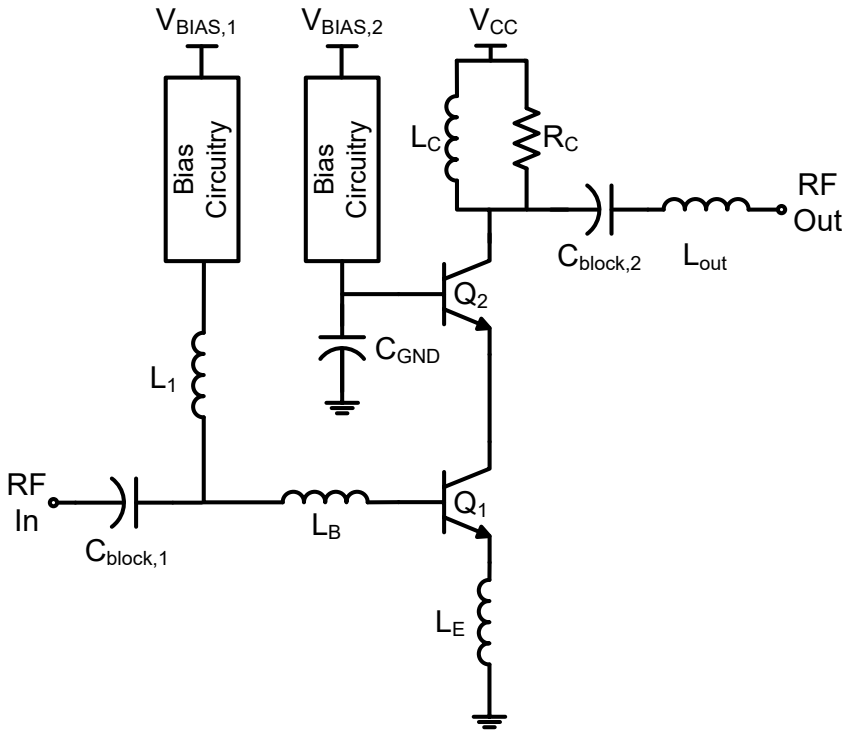

Figure 18: Schematic view of high P_{1dB} SiGe HBT LNA operating in X-band

3.5.1 Circuit Analysis

This LNA is designed in IHP 0.25-µm SiGe BiCMOS process technology which offers three types of HBTs including high performance, high voltage and low voltage characteristics. In order to meet low noise and high linearity requirements, a hybrid solution is utilized for CE and CB sub-stages. The LNA designed in a conventional inductively degenerated cascode topology. Figure 18 represents the utilized circuit configuration for the design of this X-Band high P_{1dB} SiGe HBT LNA.

During the designing process of this LNA, the methodology that is explained in the beginning of this chapter is principally followed. As mentioned before NF of the LNA is mainly determined by the CE stage and there is an inverse proportionality among f_T and NF performance of the transistors. Thus, CE core is designed via high speed HBTs with f_T/f_{max} of 110/180 GHz. In addition, simultaneous power and noise matching is also performed at the input side in an attempt to have low NF and sufficient RL across X-Band.

Since high speed HBTs have a limited collector-to-emitter breakdown voltage of only 2.3 V, variety of design considerations are performed for the aim of obtaining high linearity. Firstly, due to previously mentioned advantages in the preceding section, a large inductor L_1 is used as RF choke to increase linearity performance of the LNA. In addition, active bias circuitries are used for biasing base nodes of both Q_1 and Q_2 for achieving more power handling capability. The P_{1dB} of an LNA configured in cascode topology, is mainly determined by output voltage swing range. Due to the necessity of high linearity performance of this LNA, Q_2 is decided to be high voltage device with a collector to emitter breakdown voltage of 4.5 V. On the other hand, in cascode topology, there is no significant gain between CB and CE stages which translates to that CE stage cannot perform enough suppression to the NF caused by the CB stage. As a result, utilization of high voltage HBTs in CB stage reflects as a drawback in NF performance of the LNA. In order to achieve high linearity, Q_1 and Q_2 devices are sized with the aim of more collector current at a cost of additional NF. Collector voltages are adjusted close to breakdown voltages in order to provide maximum possible voltage swing for the RF signal. At the output, an inductor L_2 is placed for both high output RL and more RF output power.

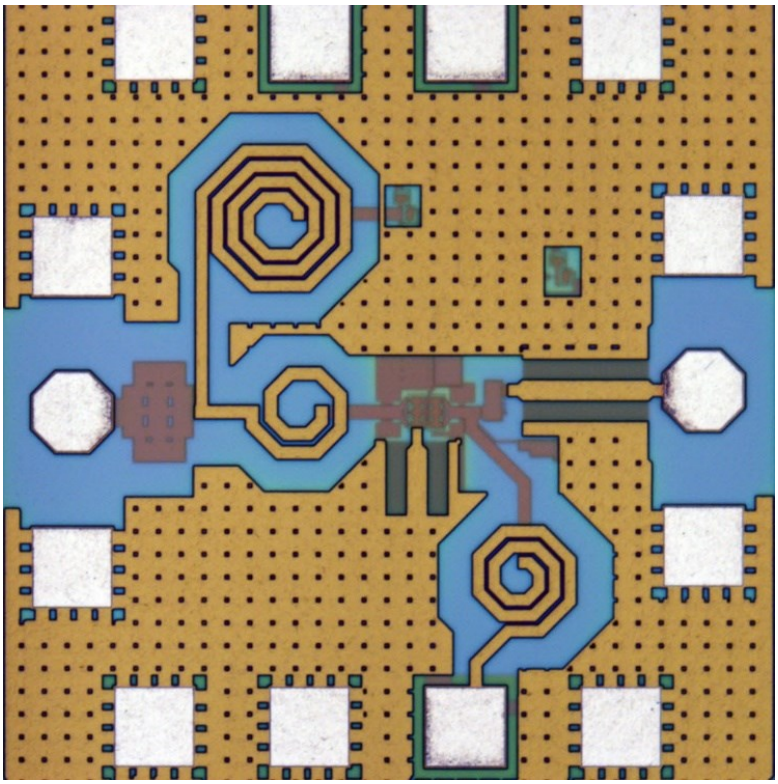

Figure 19: Die photo of the measured X-band high output power SiGe HBT LNA

3.5.2 Measurement Results

In this project, IHP 0.25-µm SiGe BiCMOS technology is employed. Figure 19 illustrates the die snapshot of the measured LNA. The chip occupies an area of 0.6 (0.75mm x 0.8mm) mm^2 including pads. The measurement process of this LNA is performed by following the methodology and using the equipment as explained in Appendix A. Biasing of the circuit is applied as the same with the simulated voltage values. Measurements show that estimated DC characteristics are exactly the same with estimated values. The die dissipates 45 mW DC power.

All the inductors and interconnections between the components are custom designed via SONNET. Inductors are placed far away from each other to diminish mutual coupling effect. In addition, the thickest and most conductive metal layer TM_2 is employed for inductor design with the intention of obtaining high Q-factor and less substrate coupling. Layout of the LNA is designed by considering parasitic effects of the components on NF, gain and linearity. For example, since high Q-factor of L_E is desired for lower NF and higher gain, the L_E is designed by utilizing

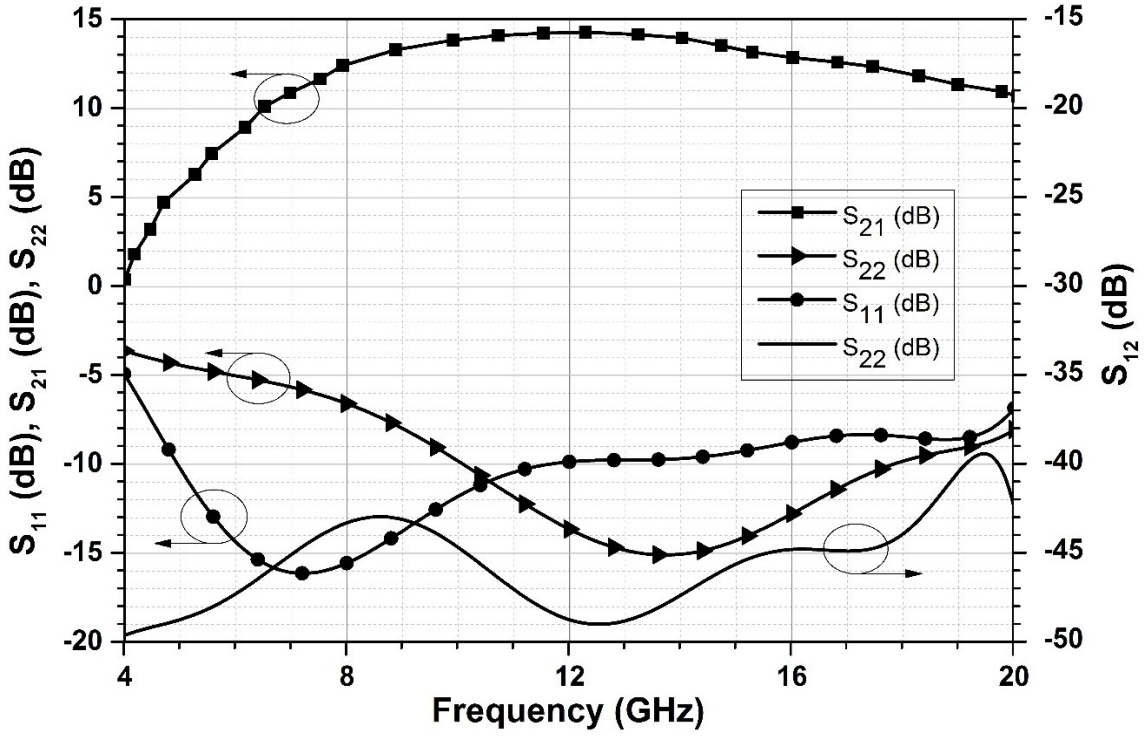

Figure 20: Measured S-Parameters of the implemented LNA

slow wave concept which provides a Q-factor more than 40. In addition, due to limited durability of the metal lines to high power levels, transistor connections are performed with wide metal lines by taking expected power flows into account. In order to reduce substrate coupling, ground plane is connected to the substrate.

The measured S-Parameters of the LNA are shown in Figure 20. As seen from the graph, input RL of the measured LNA is more than 10 dB between the frequencies of 5-14 GHz while it is at least 10 dB across X-band frequencies. The measured output RL is higher than 10 dB from 10 GHz to 20 GHz frequencies where it is at least 7 dB in X-Band. The gain of the LNA has the peak value of 14.5 dB at 12 GHz where 3dB gain bandwidth ranging from 7.5 GHz to 18 GHz. The LNA exhibits a wide band operation with acceptable RL, gain and S_{12} characteristics which makes it suitable to be used as an inter-stage amplifier in the designed T/R module. Moreover, the reverse isolation is more than 40dB between the frequencies of 2-19 GHz.

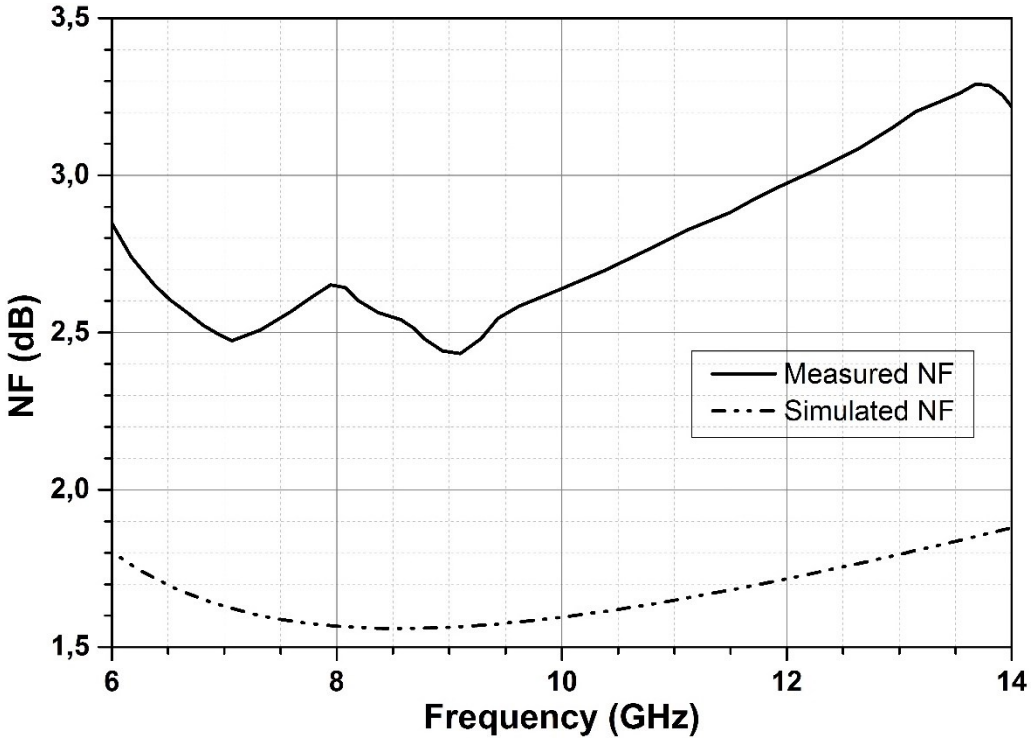

Figure 21: Measured NF performance of the LNA

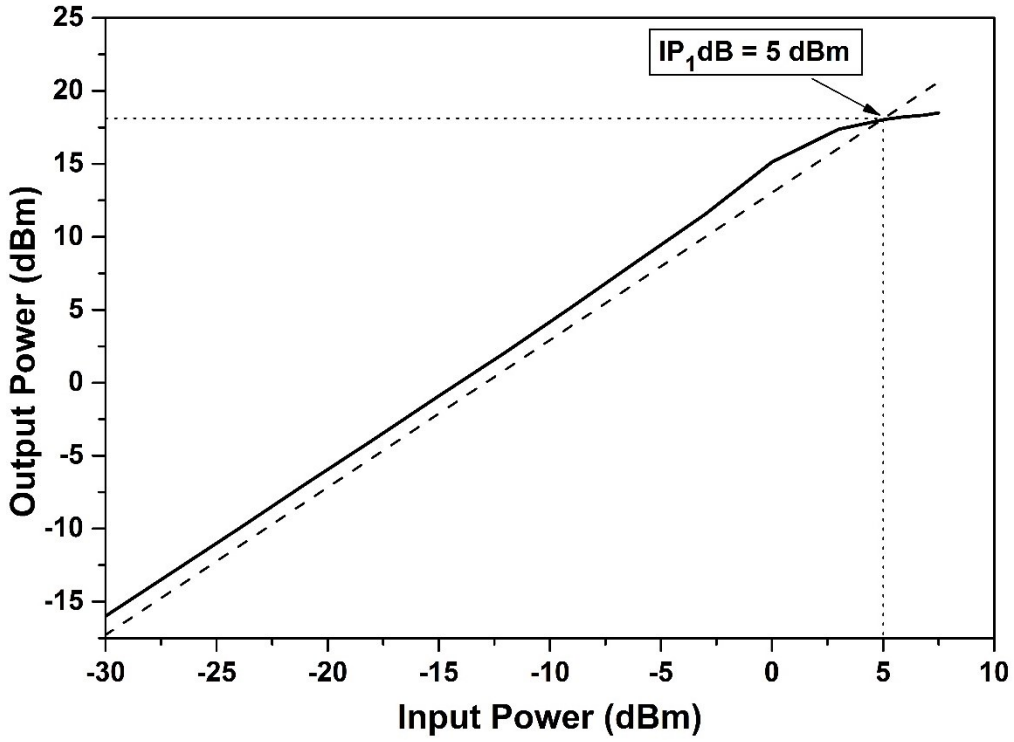

Figure 22: Measured P_{1dB} of the LNA

For a highly linear LNA, possessing a good reverse isolation is the key specification for unconditional stability which prevents the block to oscillate despite the very high output signal power of more than 18 dBm.

The NF performance of the LNA is shown in Figure 21 including both measured and simulated values. According to measured results, the LNA has an NF of 2.5 dB at the frequency of 10 GHz but it reaches to 3dB at 12 GHz. As seen from the graph, the measured NF is higher than the simulated one. This is caused by the parasitic resistance and distortion in the noise matching. Despite the high NF, the designed LNA is employed during the implementation of the T/R module by virtue of its gain, linearity and wideband operation.

Figure 22 represents input referred 1 dB compression point of the LNA. IP_{1dB} of the LNA is 5 dBm where, consequently, output P_{1dB} is measured as 18.5 dBm. In spite of the limited breakdown voltages of the HBTs offered by utilized IHP 0.25-µm SiGe BiCMOS technology, achieving this linearity performance with relatively low DC power dissipation is the main superiority of this LNA over the similar work reported earlier in the open literature.

3.6 An X-Band High Dynamic Range 2-Stage Cascode LNA

Although, the previously mentioned X-Band high P_{1dB} SiGe HBT LNA demonstrates a good performance in power handling capability, it lacks in terms of NF and gain specifications to be used as the LNA of the designed T/R module. Therefore, an LNA with higher gain and lower NF is designed for meeting high performance requirements of the T/R module for phased array radar applications. A very high gain and low NF is achieved for suppressing the NF of the following blocks in the T/R module and set its overall NF to desired level, which significant for phased array radar systems to achieve good sensitivity.

This section presents the design and implementation of a 2-stage low noise and highly linear LNA utilizing inductively degenerated cascode topology. IHP 0.25-µm SiGe BiCMOS is employed for the realization of the LNA. High performance HBTs are utilized as Q_1, Q_2 and Q_3 where the Q_4 is medium voltage HBT.

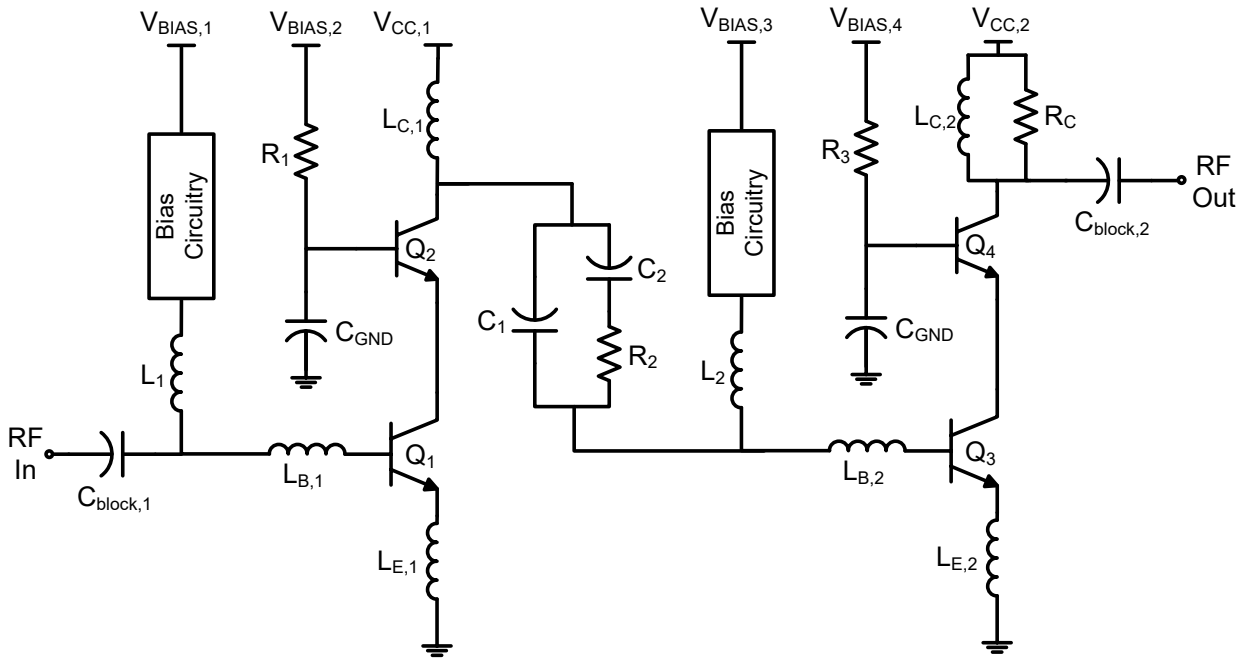

Figure 23: The schematic view of 2-stage Cascode High P_{1dB} LNA

3.6.1 Circuit Analysis

This LNA is also designed by using IHP25H3 0.25µ SiGe BiCMOS process technology. In multistage circuits, NF of the whole system is determined by initial blocks while the linearity of the system is set by the blocks at the back end. Therefore in this LNA, the first stage is designed for obtaining minimum NF while second stage is optimized for exhibiting high P_{1dB}. Figure 23 represents the schematic view of designed 2-stage cascode high P_{1dB} LNA.

For the first stage, design methodology in the section 3.2 is followed. High performance HBTs are selected for their higher f_T, which results in lower NF. Base biasing of the device Q_1 is applied by active bias circuit while considering optimum NF performance. Emitter length of the Q_1 is also adjusted for minimum NF. Moreover, gain of the first stage is designed to be high in order to suppress the noise added by the second stage. Moreover, as an RF choke, the inductor L_1 is employed for achieving a higher IP_{1dB} at the cost of narrower band input RL. Input impedance is matched to 50Ω however, output matching is set to a lower value for the aim of preventing reduction in output signal power reasoned by voltage clipping. The components C_1, C_2 and R_2 are

utilized for decreasing Q-factor of the inter-stage impedance matching network in order to prevent instability in the LNA triggered by impedance mismatch.

In the second stage, prime concern is to obtain the highest possible power handling performance at the cost of higher DC power consumption. Therefore, in the CB stage medium voltage HBTs are employed. In addition, device sizes are scaled for higher collector current resulting in higher DC power consumption of the second stage. The RF choke at the base of Q_3 is selected as an inductor (L_2) instead of a resistor with the intention of previously mentioned advantages. NF is not taken into consideration while setting the bias points of the devices. A larger emitter inductor ($L_{E,2}$) is employed for higher linearity performance while sacrificing from the gain. The output impedance is matched to 50Ω while the input impedance is set to conjugate of the output impedance of the first stage, to provide the lowest possible loss and maximum power transfer.

3.6.2 Post-Layout Simulation Results

In this project, IHP 0.25-µm SiGe BiCMOS technology is employed for the design and simulation of the LNA. Figure 24 illustrates the layout view of the LNA. The layout occupies an area of 1 (1.215mm x 0.82mm) mm^2.

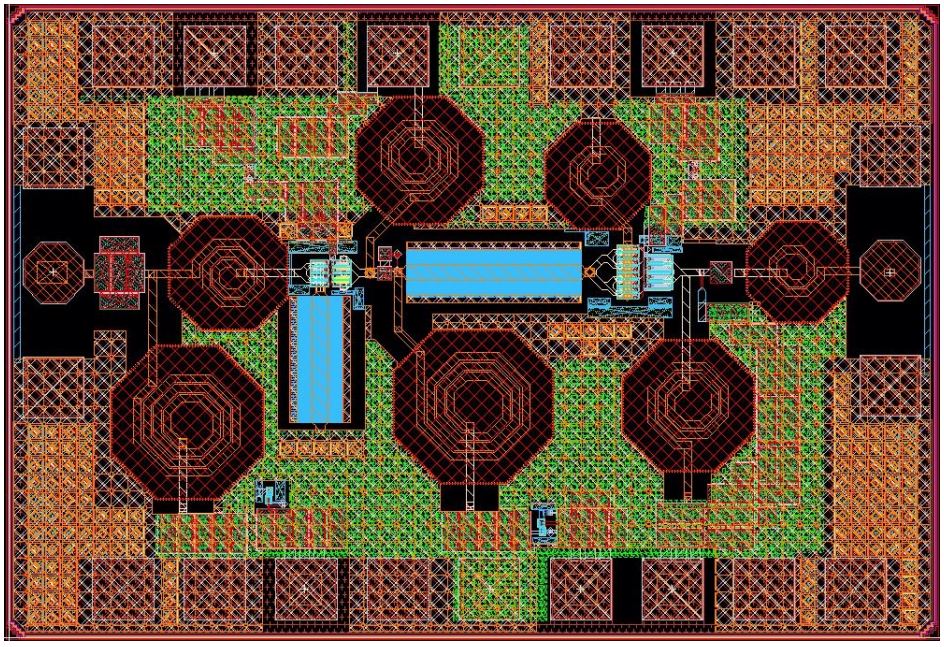

Figure 24: View of the designed LNA layout

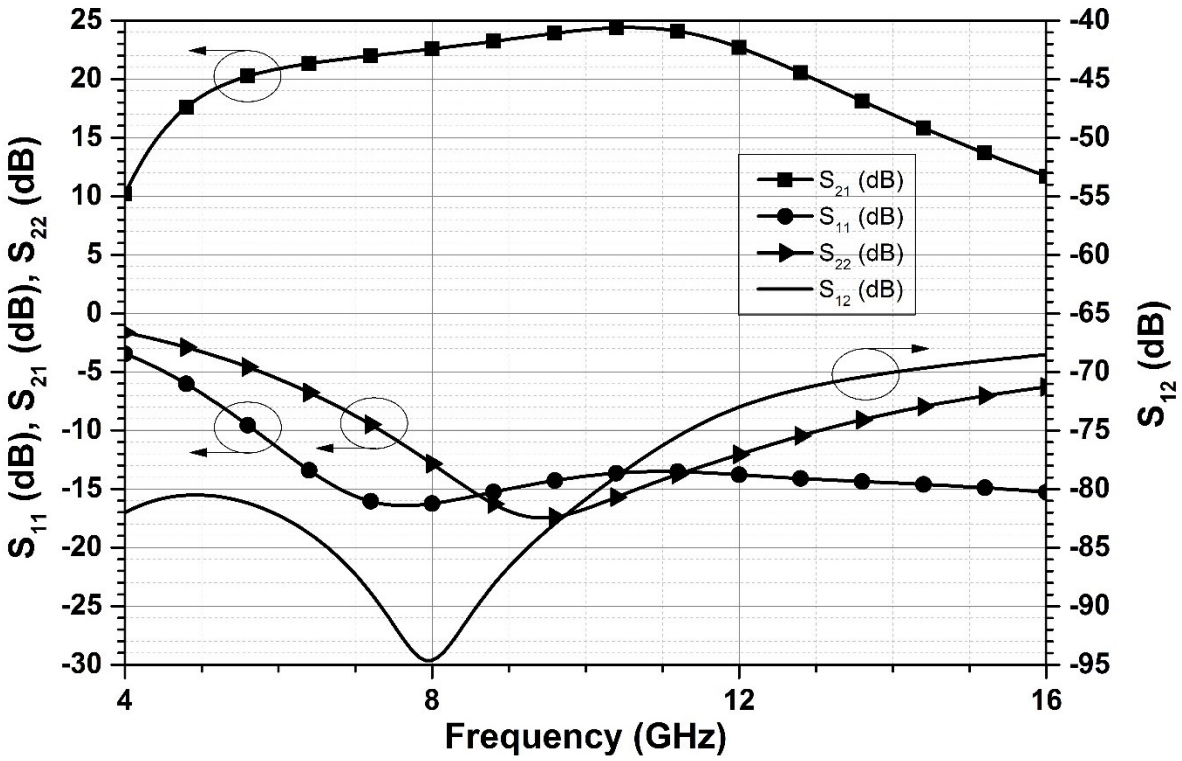

Figure 25: Simulated S-Parameters of the LNA

All the layout design considerations as previously explained for LNAs are also valid and employed during the layout of this LNA.

Simulations are performed with the *av_extracted* version of the layout including RC parasitic effects of the components as well as substrate coupling issues. Since Cadence does not run EM simulation, SONNET is employed for extracting magnetic effects of the metal lines and mutual coupling of the inductors. In order to perform a realistic simulation all the inductors are placed on SONNET and simultaneously simulated.

Figure 25 represents simulated S-Parameters of the designed LNA. As seen from the graph, the LNA exhibits a high gain that is 24 dB at 11 GHz while having a minimum value of 22.5 dB at 8 GHz. The gain of this LNA is much higher than the previous LNA as a result of employing a 2-stage topology. The input RL is greater than 10 dB starting from 5.5 GHz and demonstrates wideband characteristics. The output RL is also higher than 10 dB in X-Band.

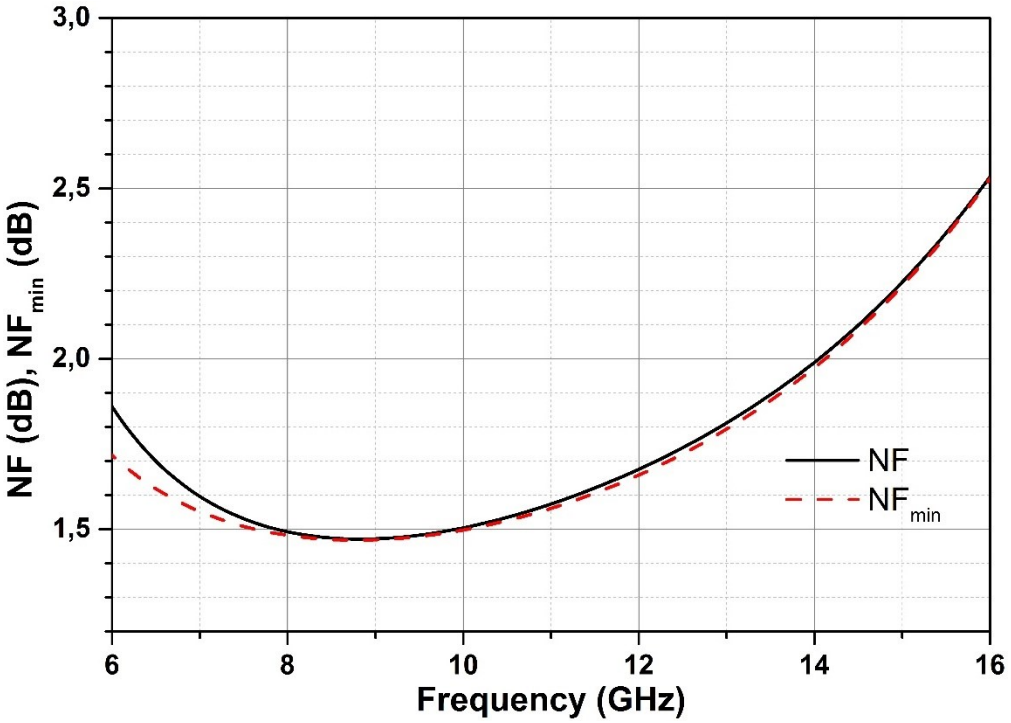

Figure 26: Simulated NF of the 2-Stage LNA

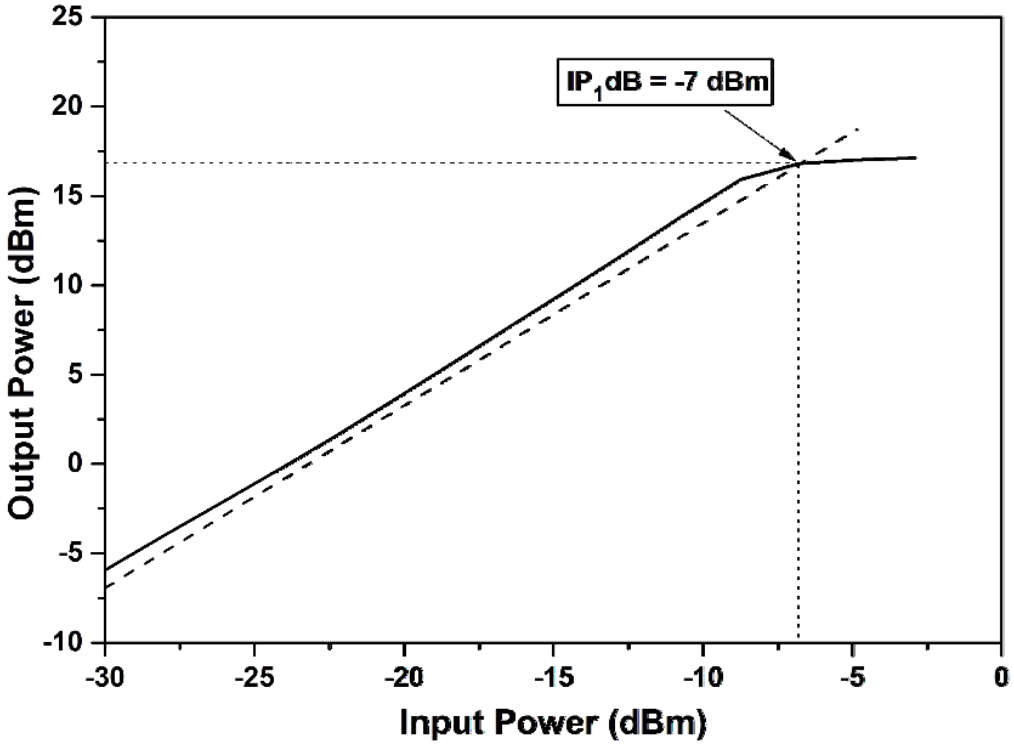

Figure 27: Simulated P_{1dB} of the designed 2-Stage LNA

The reverse isolation of the LNA is also very high as it is more than 65 dB between 4-16 GHz. The simulated NF and NF_{min} are illustrated in Figure 26. As seen from the graph, the LNA has relatively low NF which is at most 1.7dB across X-band. The NF_{min} and NF curves are almost perfectly matching which translates to that noise matching of the LNA is well performed. Figure 27 represents simulated P_{1dB} of the 2-Stage LNA. The LNA demonstrates IP_{1dB} of -7 dBm at 10 GHz.

3.7 Benchmarking

This section includes comparison of the designed X-band high 1-dB compression point SiGe HBT LNA and X-band high dynamic range 2-stage Cascode LNA with similar work available in the open literature. Table II represents performance specifications of the designed LNAs and other work implemented in 0.25µ SiGe BiCMOS technology. In order to compare performances of the LNAs the figure-of-merit (18) has been used.

Table II: Performance Comparison with the other 0.25-µm SiGe HBT LNAs in the Open Literature

Technology	**2-Stage LNA**	**1-Stage Hi. P_{1dB}**	[38]	[39]	[40]	[31]
Frequency	8-12 GHz	10 GHz	8-12 GHz	8-12 GHz	2-12 GHz	8-12 GHz
Noise Figure	1.7 dB	2.4 dB	1.65 dB	1.62 dB	3.2 dB	2.8 dB
Gain	23 dB	13.5 dB	21 dB	11 dB	20 dB	10 dB
IP_{1dB}	-7 dBm	5 dBm	-19.5 dBm	-6 dBm	-23 dBm	-24 dBm
Power Cons.	70 mW	45 mW	22 mW	18.6 mW	78	2 mw
Die Area	0.99 mm^2	0.61 mm^2	0.5 mm^2 (*)	0.3 mm^2 (*)	0.16 mm^2	0.56 mm^2
FoM	**13**	**11.4**	0.55	1.48	0.039	0.13

(*): Pads are excluded

4. A Reverse-Saturated SiGe HBT T/R Switch based on Slow Wave Tx-Line

The designed T/R module aforementioned in chapter 2, consists of three SPDT switches. One of SPDT switches serves as T/R switch while the remaining ones are required for routing the signal in a way that allows utilizing common attenuator and PS circuits in both receive and transmit modes of T/R module. IHP 0.25-µm SiGe BiCMOS technology is employed for the realization of the designed T/R switch.

This chapter presents design and implementation of a T/R switch which combines several techniques such as reverse saturation method, DC bias of the signal path and quarter-wave-length slow wave based transmission lines in order to provide low IL, high power handling capability and smaller area occupation. Generally, T/R switches demonstrate high linearity but on the other hand, they also exhibit high IL. Therefore, individual designs would be required for SPDT and T/R switches in the 7-bit T/R module. However, the designed SPDT operates with both very high power handling capability and low IL.

4.1 Introduction

The RF single-pole double-throw (SPDT) switches can be employed in various applications such as attenuators (Figure 28 (b)), phase shifters (Figure 28 (c)), wideband pulse generators, multi-standard communication systems and T/R modules [41]. Utilization of T/R switch in a T/R module provides compactness to the system by allowing the use of a single antenna for both transmit and receive in the time division duplexing (TDD) based front-end [42]. Without a T/R switch, two separate antennas should be utilized for transmitter and receiver, which causes reduction in antenna gain and aperture size for a given area [43]. As a result, T/R switches are one of the most essential blocks for T/R modules for phased array applications in which the area and cost of each element should be kept minimum. As a consequence of their location and function in a T/R module (Figure 28 (a)), performance of T/R switches plays a significant role in overall system characteristics. In many examples, T/R switch interfaces with three different and important circuit blocks which are the LNA, PA and RF antenna [44].

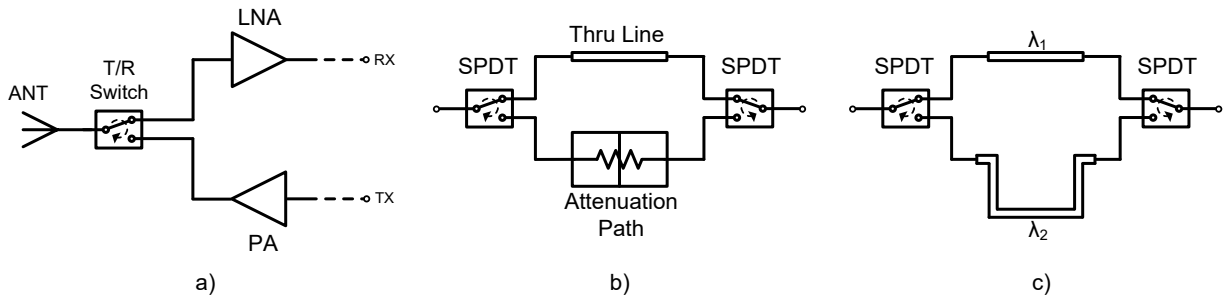

Figure 28: Utilization areas of SPDTs in a) T/R modules b) attenuators c) phase shifters

The main roles of the T/R switch in a transceiver system is routing the input signal received by the antenna to the LNA and conducting the output signal amplified by the PA to the antenna. In all designs, T/R switches must exhibit high isolation, low IL and relatively high power handling capability [45].

A high isolation between Rx and Tx nodes of T/R module is a highly desired design specification because high power output signal of the PA has to be directed only to the antenna while being attenuated towards receive path for higher transmission efficiency. In transmit mode, any leakage of signal towards the more sensitive receiver side may cause cross-talk and instability problem.

A low insertion loss (IL) is also a critical performance parameter of a T/R switch because at the receiving side, the incident signal is exposed to IL of the T/R switch which results in direct contribution of this loss to the overall system NF. Moreover, an increase in NF results to reduce input SNR, which causes degradation in the sensitivity and directivity performance of phased array radar. On the other hand, during the transmit mode of operation, IL of the T/R switch reflects as a decrease in maximum output power which correlates to a reduction in transmission efficiency of the radar.

Since the T/R switch is placed right after a PA, during the Tx mode, T/R switch has to be able to handle high power input signals injected by the PA. Therefore, linearity is also an important performance metric that must be taken into account during the design of a T/R switch to maintain

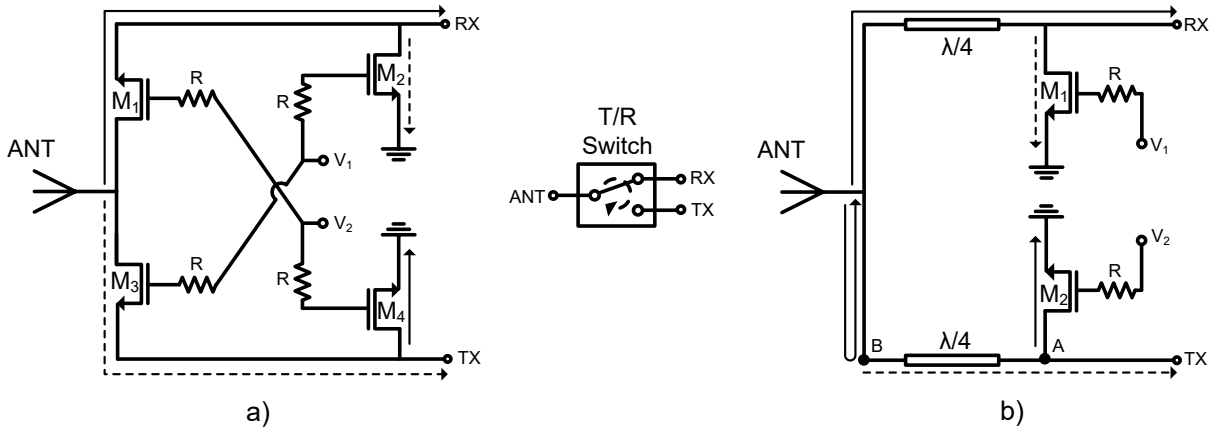

Figure 29: Circuit topology of a) absorptive type, b) reflective type T/R switches

high transmission efficiency and reliability of the system. For the receiver side, linearity performance of the T/R switch is not a bottleneck because input signal power will never reach to such level that may saturate the T/R switch.

4.2 T/R Switch Architectures

SPDT switch circuit topologies can be generalized into two main categories namely absorptive type and reflective type. Both topologies have particular advantages and drawbacks depending on the frequency band of interest, design specifications, area, cost or technology limitations as well as application specific issues.

The name absorptive derives from the approach for eliminating the power leakage from antenna to transmit node or transmit node to receive end. In this topology, undesired power leakage to a node is cancelled by absorbing the signal by the resistive attenuation of a series connected switch operating in off state or grounding the signal with a turned on shunt switch. Figure 29 (a) represents circuit topology of a conventional absorptive type T/R switch in receiving mode ($V_1<V_{th}<V_2$) utilizing FET based switches. Preferred power flow paths are depicted by arrows while undesirable signal leakages are shown via dashed lines.

In the absorptive type series-shunt T/R switch topology, the signal flows through the device M_1 and reaches to receiving end while an IL is applied by R_{on} resistance of M_1 and C_{off} capacitance of M_2. On the other hand, a signal leakage which degrades the isolation performance, occurs

through the C_{off} of M_3. This leakage is grounded by R_{on} resistance of M_4 for improving isolation performance of the T/R switch. In all the switches, lower C_{off} and R_{on} values are required for high isolation and low IL. However, R_{on} changes inversely proportional to device size while C_{off} shows direct proportionality. Therefore, there is a trade-off between isolation and IL performances, which requires careful scaling of devices in order to have optimum R_{on} and C_{off} values. This T/R switch structure is generally chosen for low frequency applications because IL of conventional shunt-series topology increases significantly at higher frequencies [46].

In the reflective type quarter wave single shunt T/R switch topology Figure 29 (b), power leakage towards an undesired node is prevented by enforcing the signal to be reflected due to high impedance created by transmission lines or lumped elements. As a result they are called as reflective type T/R switches.

As seen in Figure 29 (b), the signal received by the antenna travels towards to the receiving node without passing through any series switch. An IL is added by the λ/4 transmission line and C_{off} of the device M_1. Since the loss of a properly designed λ/4 transmission line is lower than a series switch, this structure exhibits less IL with respect to series shunt topology. At the transmitter side, the signal reflects back from the node B because an approximate ground impedance created by the turned-on device M_2 at node A is transformed to a very high resistance by λ/4 transmission line at B. However, due to finite impedance at node B, a portion of signal leaks towards the Tx node which translates to decrease in isolation performance of the T/R switch. This topology is usually utilized for high frequency applications due to their lower IL. Moreover, the large size of λ/4 transmission lines, prevents this configuration to be employed in low frequency applications due to area constraints.

4.3 Circuit Design and Analysis

In this section, design and implementation of a fully integrated reflective type SPDT switch operating in X-Band is presented. The switch is based on a quarter wave double shunt switch topology utilizing SiGe HBT devices. Figure 30 illustrates the schematic view of the designed SPDT switch in receiving mode.

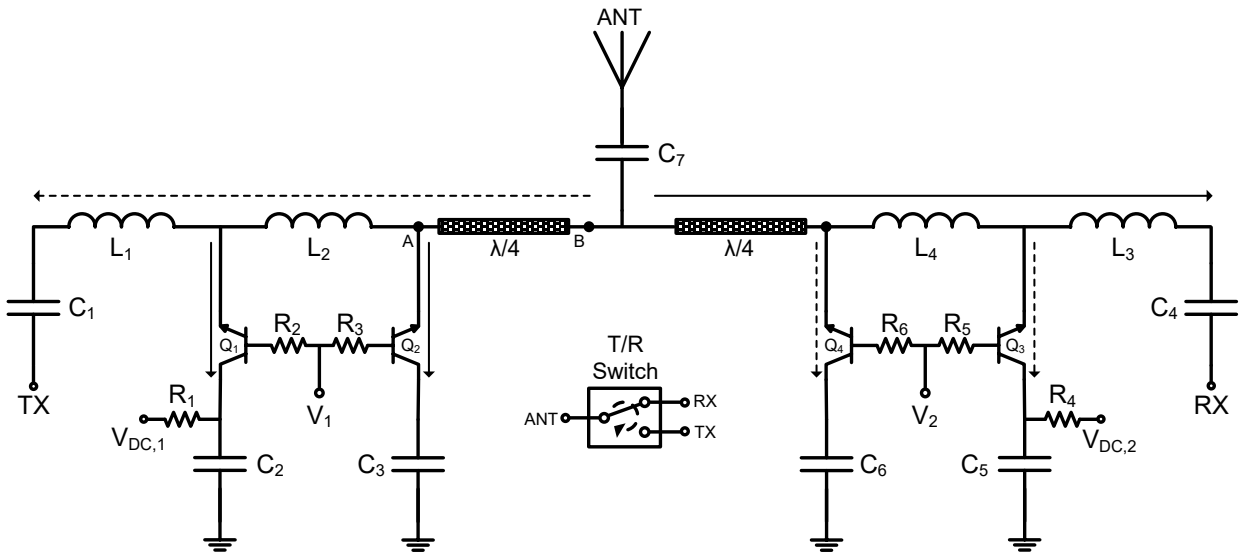

Figure 30: The schematic view of designed T/R switch

In order to enable the use of the same SPDT as also a T/R switch, low IL, very high isolation and power handling capability are main design considerations.

When 5V is applied as V_1 while V_2 is 0 V, received signal by the antenna is routed to Rx side with the insertion losses of quarter-wave transmission line and C_{off} capacitances of Q_3 and Q_4. SiGe HBTs are employed instead of FET based devices due to their lower C_{off} at the cost of additional DC power consumption. Moreover, HBTs are connected as shown in Figure 30 for utilizing advantages of reverse saturation mode that will be explained in following section. Internal parasitic resistances of L_4 and L_3 are also contributing factors for more IL. Utilizing two shunt switches causes additional IL for the system. Therefore, L_4 is used to resonate out parasitic capacitances of Q_3 and Q_4 devices to reduce IL whereas L_3 serves as a part of impedance matching. Resistors R_5 and R_6 are employed for preventing power loss through Cπ capacitances of the HBTs, which also translates to lower IL.

For the Tx side, double shunt switches are placed for providing better isolation by blocking the signal with both reflecting (Q_2 and λ/4) and absorbing (Q_1) approaches. Due to the symmetry of the device, all design and operating issues are also valid for the transmit mode.

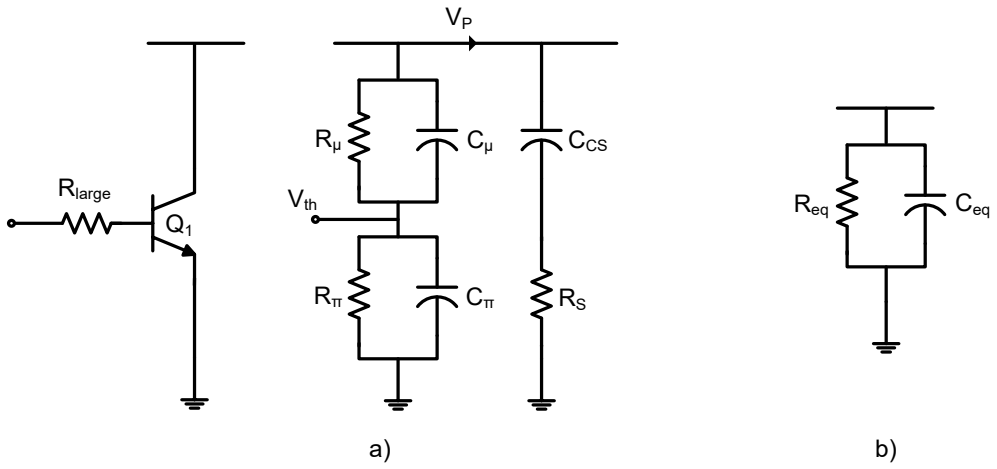

Figure 31: Capacitive model of an HBT switch

Since the designed T/R switch operates in X-Band, placing a conventional λ/4 transmission line requires large area. Even in the mm-wave frequencies λ/4 lines are too bulky and requires too much area to be implemented on a chip [43]. Hence, slow-wave approach is utilized for the design of λ/4 transmission lines and chip area is reduced.

4.3.1 Analysis of SiGe HBT Switches

The designed SPDT is composed of a quarter-wave transmission line utilizing slow-wave approach and four shunt switches with the help of other lumped components to achieve improved performance parameters. CMOS transistors and *pin* diodes would be employed for the design of switches. The main limitation for utilizing CMOS transistors in switch design is their large parasitic junction diodes between source-drain and substrate [47]. Furthermore, *pin* diodes require high bias current and cause high IL as a switch [48]. Performance of a series or shunt switch can be evaluated by following figure of merit (FoM):

$$FoM = \frac{1}{R_{on} * C_{off}} \tag{19}$$

As seen from (19), a high performance switch must exhibit low R_{on} and C_{off} in order to achieve low IL and high isolation. In a turned on switch R_{on} dominates the total impedance of the switch while in turned off state, R_{off} and C_{off} are both effective. Figure 31 (a) represents capacitive model for a switch designed using HBT. C_{CS} indicates collector-to-substrate capacitance whereas

R_S refers to substrate resistance. Under the conditions assuming that Rπ is equal to Rμ and Cπ has the same value as Cμ, the total model reduces to parallel RC network shown in Figure 31 (b). Req and Ceq can be formulated as following [49]:

$$R_{eq} = \frac{2R_\pi\left[1+\left(\omega R_S C_{CS}\right)^2\right]}{1+\left(\omega R_S C_{CS}\right)^2\left[1+\left(\frac{2R_\pi}{R_S}\right)\right]} \tag{20}$$

$$C_{eq} = \frac{C_\pi}{2} + \frac{C_{CS}}{1+\left(\omega R_S C_{CS}\right)^2} \tag{21}$$

When the switch is turned-on $R_S >> R_\pi$. Under this condition $R_{eq,on}$ can be calculated as:

$$R_{eq,on} = \frac{2R_\pi\left[1+\left(\omega R_S C_{CS}\right)^2\right]}{1+\left(\omega R_S C_{CS}\right)^2} \approx 2R_\pi \tag{22}$$

As seen from (22), R_π is the prime factor for determining the R_{on} of the switch which translates to reverse proportionality between the emitter length of the HBT and IL of the switch. When the switch is turned-off, $R_\pi >> R_S$. $R_{eq,off}$ can be calculated as:

$$R_{eq,off} \approx R_S + \frac{1}{\omega^2 R_S C_{CS}^{\ 2}} \tag{23}$$

Equation (21) and (23) indicate that higher substrate resistance leads to lower IL and greater isolation for the T/R switch. As mentioned earlier, power handling capability of a switch which is evaluated by 1-dB compression point, is also an important specification for T/R switch. Power handling of a switch is limited by the voltage created at base/gate of the transistor due to self-biasing effect [50]. If the capacitive switch model shown in Figure 31 (a) is analyzed, half of the voltage of incident signal drops to the base of the HBT due to equivalence of C_π and C_μ. Consequently, if Vp/2 reaches to Vth, the device turns on and a low loss path is created from RF signal line to the ground, which results in power loss. Therefore, RF power level that enforces the off-state HBT to turn on is expressed as [49]:

$$P_{1dB_{\min}} = \left(\frac{2V_{th}}{\sqrt{2}}\right)^2 \frac{1}{Z_0} \tag{24}$$

Equation (24) indicates that a switch designed with higher threshold voltage devices demonstrates more power handling capability. Nonetheless, generally high voltage devices has a drawback in terms of high internal capacitances and high R_{on} which cause more IL. There are also SPDT designs that employ multiple switches stacked together [48]. This approach leads to improvement in P_{1dB} by the square of number of switches (n^2).

4.3.2 Reverse Saturation

In this T/R switch design SiGe HBTs operating in reverse-saturation mode are utilized to design shunt switches. As seen from Figure 30, collector of the SiGe HBT is connected to ground while emitter node is placed on the signal path.

Figure 32 illustrates energy band diagram of a SiGe HBT in equilibrium condition where ΔE_{EB} and ΔE_{CB} indicate energy needed for an electron to transport from emitter to base and collector to base, respectively. As seen from the diagram, ΔE_{EB} is much greater than ΔE_{CB} due to higher doping level of the emitter and graded Ge doping across the base, which corresponds to that an electron experiences a larger barrier to transport from emitter to base [51].

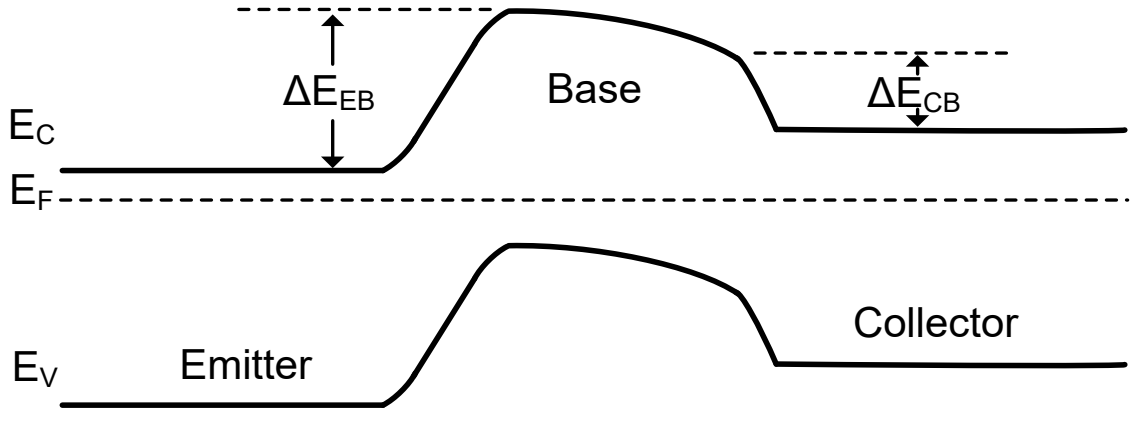

Figure 32: Energy Band Diagram for SiGe HBT in equilibrium

When an HBT switch is in off-state, the device has the same energy band structure as shown in Figure 32 which translates to that signal leakage is lower in the configuration where emitter node is connected to RF signal path and collector is grounded. A reverse saturated HBT achieves approximately eight times greater $R_{eq,off}$ resistance as compared to other configurations [49]. Consequently, utilizing reverse saturation mode of an HBT significantly improves IL performance of a T/R switch.

In addition, due to the geometry of the device, physical isolation of the emitter from the substrate is better with respect to the isolation of collector [51]. Therefore, emitter to substrate junction capacitance is smaller than C_{CS}, hence, power leakage towards the substrate is also lessened by the use of reverse saturation method. As a result, employing reverse saturated HBTs in T/R switch design decreases IL by increasing $R_{eq,off}$ as well as minimizing junction capacitances.

4.3.3 λ/4 Transmission Line Based on Slow Wave Concept

The designed X-band T/R switch is the first sample that combines slow wave transmission line concept with the utilization of reverse saturated HBTs in SiGe BiCMOS technology. As mentioned before, conventional λ/4 transmission lines are too bulky and require substantial area for implementation on a circuit operating in X-band. In order to decrease area occupation of transmission lines in the designed 7-bit T/R module, slow wave structure is employed.

In the design of slow wave transmission lines TM_1 and TM_2 metal layers which are the thickest and the most conductive metals for realizing RF signal path are employed, while M_3 layer is chosen for constructing slotted bottom ground shield. Slow wave approach significantly decreases the size of the transmission line for achieving a quarter-wave electrical length. The wavelength of signal propagating through a transmission line (λ_{Tx}) can be expressed as (25) where L and C are inductance and capacitance per unit length, respectively:

$$\lambda_{Tx} = \frac{1}{f\sqrt{LC}} \tag{25}$$

As seen from (25) increasing f, L and C decreases wavelength of the signal in the transmission line. Since the operating frequency is fixed (X-band), only L and C can be modified

for lower λ_{Tx}. However, while adjusting L and C, their ratio has to be kept constant due to maintain 50Ω characteristic impedance ($Z_0 = \sqrt{L/C}$).

In consequence of using slow wave transmission lines, IL of the T/R switch decreases because parasitic resistance of a shorter transmission line is lower than the conventional one. In addition, provided by the slotted ground shield covering the bottom side of the transmission line, substrate coupling is reduced.

4.3.4 DC Biasing of the Signal Path

As mentioned before, IL of the T/R switch is mainly determined by parasitic junction capacitances (C_{off}) and R_{off} of the shunt switches. Consequently, lowering C_{off} leads to a decrease in IL of the system. In the designed T/R switch, for the aim of decreasing junction capacitances, DC bias is applied to collector and emitter of the HBTs which widens depletion region and provides smaller junction capacitances.

In addition, applying a reverse bias to collector and emitter causes the HBTs to be turned on at higher voltages, which translates to higher power handling capability for the T/R switch. Hence, very high P_{1dB} value is obtained, will be shown later.

DC bias of the T/R switch is applied from voltage sources $V_{DC,1}$, $V_{DC,2}$ as shown in Figure 30. In order to limit current flow and eliminate inductive effects of wire bonds, the resistors R_1 and R_4 are connected as illustrated. The large capacitors C_2, C_3, C_5, and C_6 are placed for keeping the RF signal path at 2V and prevent short circuit to the ground. Moreover, capacitors C_1, C_4 and C_7 are used for DC signal flow towards the RF pads.

4.3.5 Post-Layout Simulation Results

IHP 0.25-µm SiGe BiCMOS technology is employed for design and simulation of the T/R switch. Figure 33 demonstrates the snapshot of the T/R switch layout. The layout occupies an area 0.93 (0.93mm x 1mm) mm^2. For the proper EM modelling of the inductors and transmission lines SONNET simulation tool is employed. The quarterwave-length Tx line is custom designed

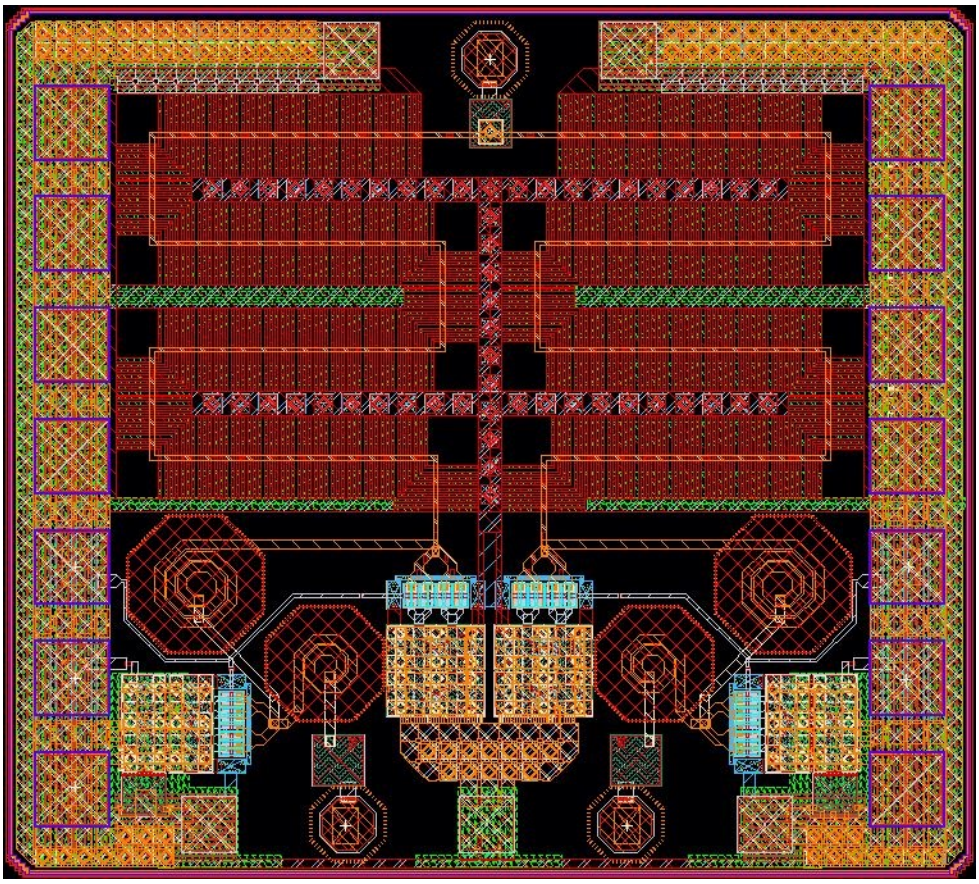

Figure 33: Snapshot of the layout of T/R switch

by using the two top metal layers TM_1 and TM_2 whereas slotted ground shield is constructed with M_3. TM_1 and TM_2 metal layers are utilized due to their superior conductivity and thickness with respect to other metal layers. The reason that M_3 is employed to realize the ground shield is its smaller distance to TM_1 and TM_2 for providing higher capacitance per length, which facilitates achieving quarter-wave electrical length with a shorter physical length. In addition, M_3 is located further away from the substrate compared to M_2 and M_1 layers which translates to less substrate coupling and loss. Since, signal path consists of two metal layers, they are connected to each with great number of vias with the intention of decreasing parasitic resistance of the transmission lines. As a result a quarterwave transmission line is designed with low loss and small area occupation. The inductors L_1, L_2, L_3 and L_4 are placed away from each other for reducing magnetic coupling effect. Nevertheless, they are all simulated simultaneously in SONNET environment.

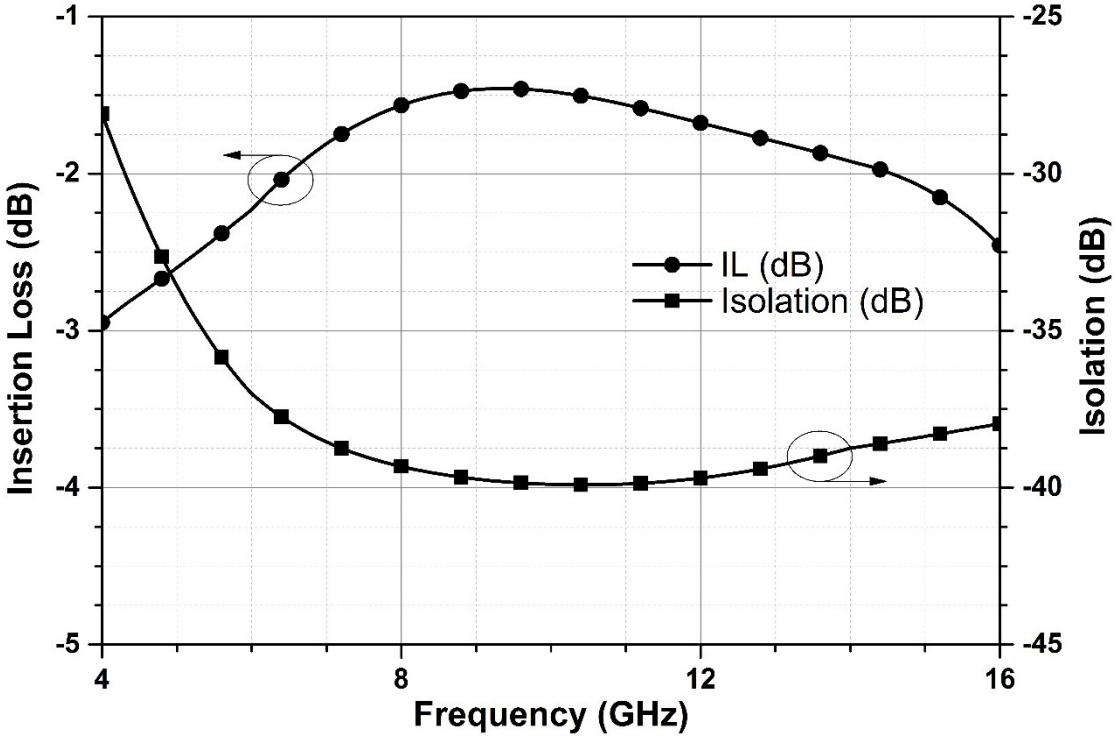

Figure 34: Simulated IL and Isolation of the designed T/R switch

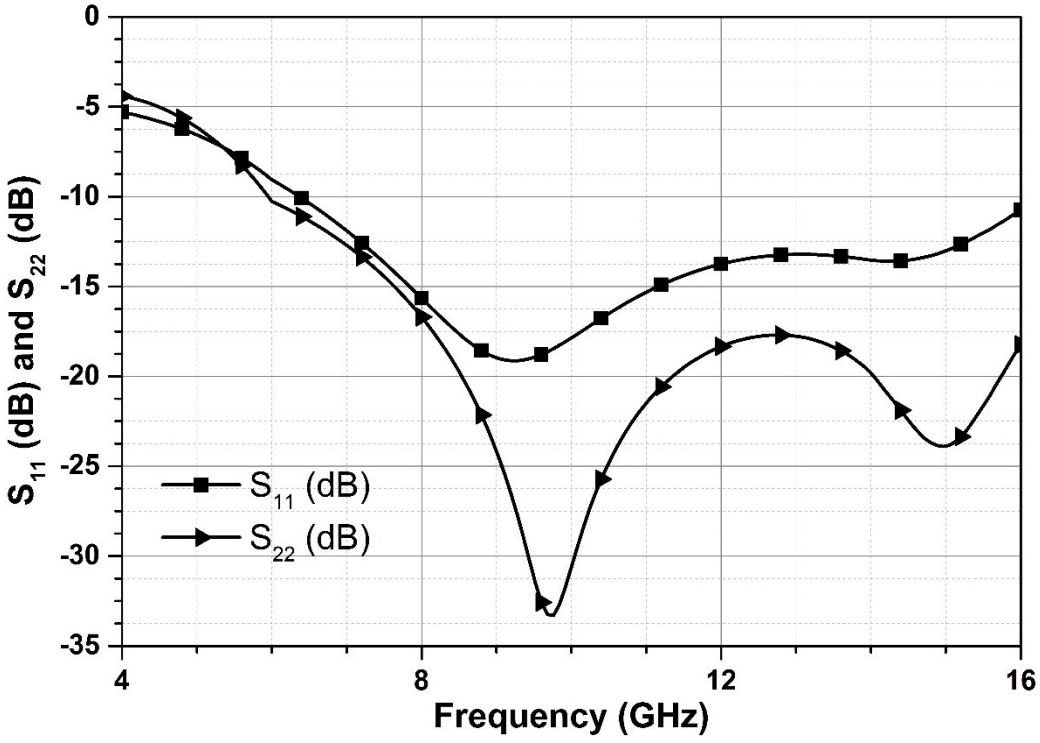

Figure 35: Simulated S_{11} and S_{22} of the T/R switch

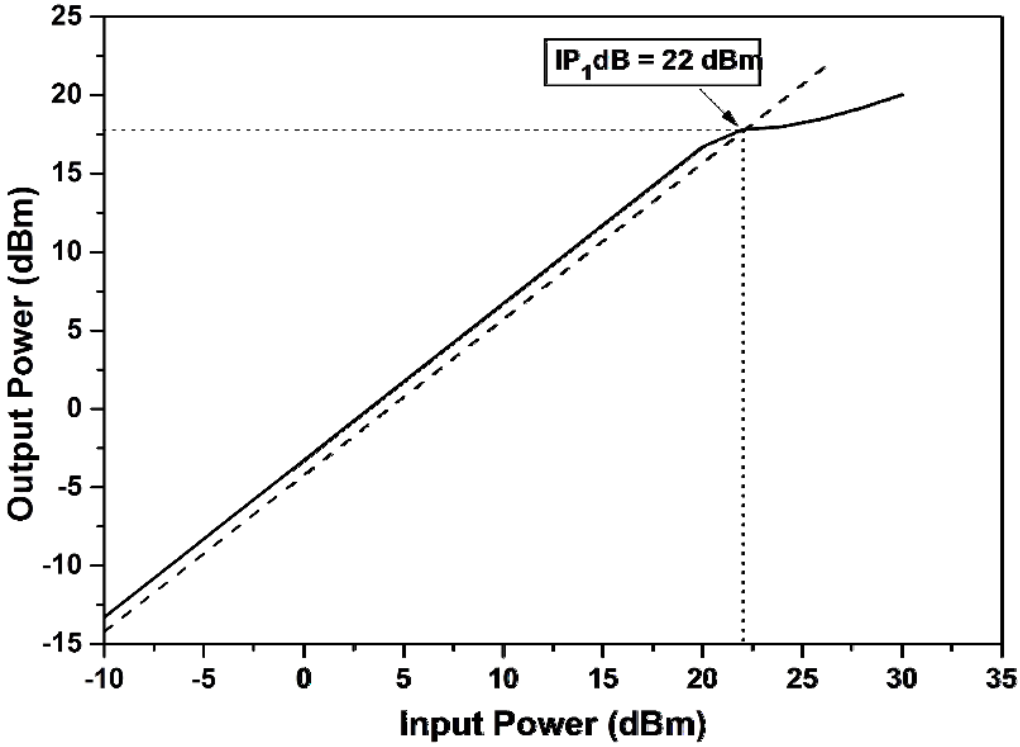

Figure 36: Simulated 1-dB compression point of the designed T/R switch

A proper construction of ground plane in a T/R switch layout is especially important for high performance because RF signal must be well grounded to provide high isolation. Therefore shunt capacitors are connected to ground by using multiple metal layers.

Figure 34 represents simulated IL and isolation of the designed T/R switch. As seen from the graph, the T/R switch exhibits a low IL of at most 1.7 dB across X-Band while the isolation is about 40dB which are good enough to achieve desired performance parameters for the designed T/R switch. RL performance of the T/R switch is illustrated in Figure 35. The graph shows that starting from 6 GHz, input and output RLs are greater than 10 dB until the frequency of 16 GHz. The simulated 1-dB compression point of the designed T/R switch is represented in Figure 36. Simulations demonstrate that input referred P_{1dB} of the T/R switch is 22 dBm.

Table III: Performance Comparison of the T/R module with Similar Work in the Open Literature

Reference	Frequency (GHz)	Technology	Isolation (dB)	IL (dB)	RL (dB)	P_{1dB} (dBm)	Die Area (mm^2)
[52]	8-12	0.2µm SiGe HBT	35-58	1.6-2.4	>9	10	0.2*
[53]	8-20	0.13µm SiGe BiCMOS	>15	1.4-2	>15	12.5	0.29*
[54]	10-18	0.18µm SiGe BiCMOS	>22	<1.9	>13	21	0.005*
[55]	DC-20	0.18µm CMOS	25-60	0.5-2.5	>9	>19.8	0.06*
[56]	8-12	0.25µm SiGe BiCMOS	>23	1.8-2.2	>20	17	0.17*
[57]	8-12	0.25µm SiGe BiCMOS	39-42	2.1-2.9	>7	27.6	0.73
This Work	**8-12**	**0.25µm SiGe BiCMOS**	**39-40**	**1.7**	**>14**	**22**	**0.93**

(*) excluding pads

4.4 Benchmarking

This section presents performance comparison of the designed reverse-saturated SiGe HBT T/R switch based on slow wave Tx-line with similar work available in the open literature. Table III represents performance parameters of the T/R module.

5. 7-Bit Digital Step Attenuators for X-Band T/R Modules

In this section, design and implementations of two types of digitally controlled 7-bit step attenuators where one of them utilizes CMOS switches while the other one employs HBTs for switching operation, will be discussed.

5.1 Introduction

In phased array radars, there are high number of transmit/receive (T/R) modules of which amplitude and phase components must be individually controlled for the purpose of beam shaping and amplitude weighting. In phased-array antenna systems and beam-forming applications, wide and accurate control of amplitude is required in order to adjust the side-lobe levels and null points of the array precisely, and low phase variation during amplitude adjustment is required to avoid tracking errors and complex phase/amplitude calibrations for phased array radar systems [58] [59].

T/R modules in a phased array RADAR system must be low power consuming because power dissipation of a T/R module is multiplied due to the use of substantial number of elements. Therefore, using passive structures for amplitude controlling purpose in a T/R module saves enormous amount of power consumption for the overall system. Amplitude control in a T/R module can be performed by both variable gain amplifiers (VGA) and attenuators. In both VGAs and attenuators variety of methods are utilized in order to decrease phase variations while adjusting signal power. Attenuators are preferred over VGAs because they don't dissipate DC power due to passive structure utilizing CMOS devices as switches. In addition, attenuators are less dependent on temperature variations while exhibiting higher power handling capability and providing more accurate phase/amplitude control in a wide range of frequency and signal power.

The design specifications of an attenuator are exhibiting low IL, high amplitude adjustment range, low RMS attenuation error and high precision. Moreover, while attenuation states are varying, insertion phase added by the attenuator must be close to a reference phase in order to obtain low RMS phase error. Power handling capability of the attenuator is also an important design specification because in a T/R module in receiving mode, incident signal amplified by the LNA is transferred to attenuator. Therefore, the attenuator has to be able to operate in high signal powers

without causing saturation at the output. Performance of the attenuator plays a significant role in overall system performance of the T/R module and consequently in phased array.

5.2 Attenuator Architectures

In the open literature, there exist three types of attenuators: switched path attenuators [60], distributed attenuators [61] and switched π/T attenuators [62]. Figure 37 represents simplified circuit illustrations of (a) switched path attenuators and (b) distributed attenuators.

Switched path attenuators employ SPDT switches in order to switch RF signal between a reference through line and a resistive network to provide relative attenuation between two paths. Switched path attenuator topology exhibits low phase variation among attenuation and reference states but IL is high due to individual losses of SPDT switches. In addition, they occupy larger die area due to use of multiple SPDT switches. Thus, for a 7-bit attenuator, switched path attenuator topology is not feasible due to bearing high insertion loss and die area constraints.

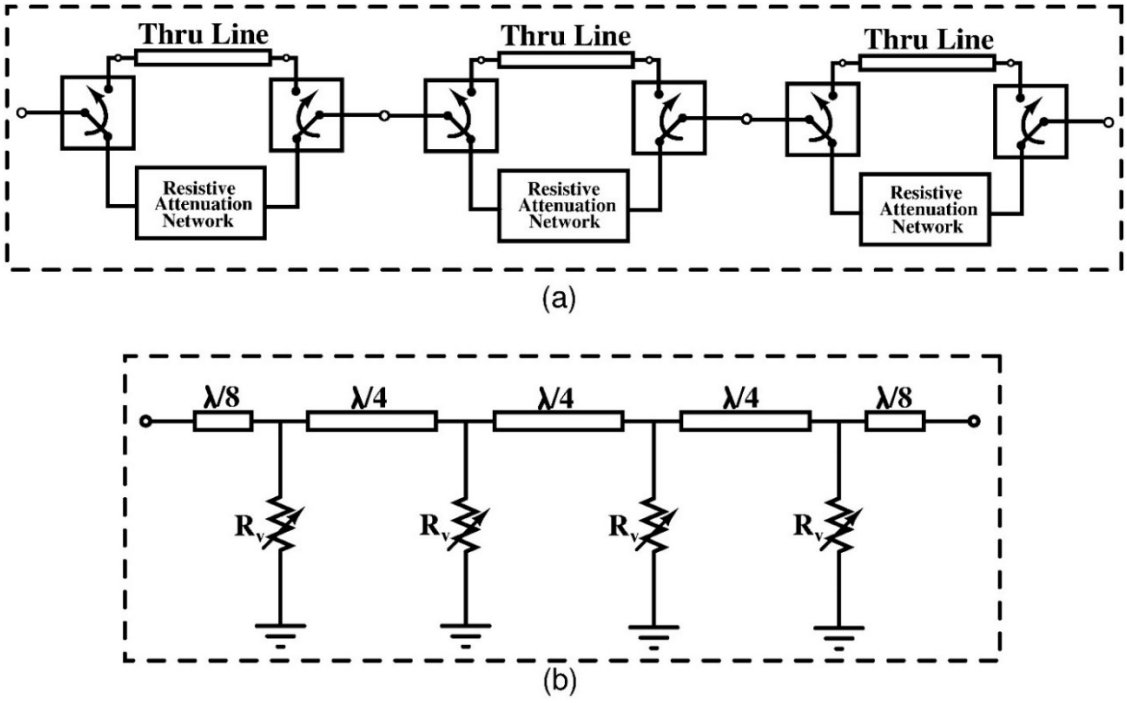

Figure 37: Simplified circuit configurations of (a) switch path, (b) distributed attenuators

Distributed attenuators are based on shunt p-i-n diodes in between quarter wave length transmission lines. The diodes are used as variable resistors or switches to short RF signal to the ground and provide attenuation while transmission lines are used for matching input and output impedances to the system impedance (50Ω). Distributed attenuators are superior to switched path attenuators in terms of IL as there are no serially connected switches in signal path. The IL applied to the incident signal is caused from internal parasitic resistances of λ/4 transmission lines and shunt parasitic capacitances introduced by the junction inside the p-i-n diodes. In addition to low IL, distributed attenuator topology provides also wideband operating frequency range. However, when the frequency of interest concerns X-band or below, quarter wave length transmission lines occupy very large area on the die. Consequently, distributed attenuator topology is not suitable to be used in an X-band 7-bit attenuator design.

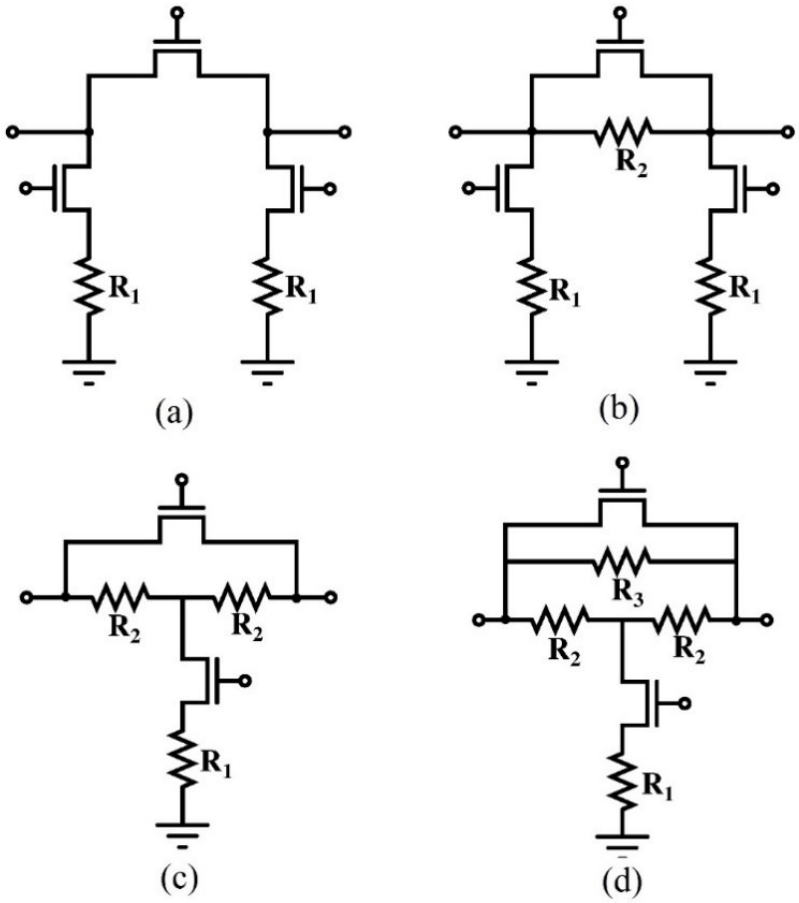

Figure 38: Π/T type Attenuator Topologies (a) Switched Π-Type (b) Bridged Π-type (c) Switched T-type (d) Bridged T-type

In this design, switched Π/T type attenuator topology has been employed because of the advantages such as wideband impedance matching, small area occupation, high linearity and enhanced phase/amplitude control compared to other topologies. Figure 38 represents circuit diagrams of conventional Π/T type attenuator topologies. Switched Π-type attenuator is illustrated in Figure 38 (a) while switched T-type attenuator is shown in Figure 38 (c). Bridged versions of both attenuator topologies are demonstrated in Figure 38 (b) and (d), respectively.

Compared to the Π-type and T-type attenuator topologies, bridged Π-type (b) and bridged T-type (d) are deficient in relative attenuation capability. However, phase variation is lower in bridged ones because there is a resistive path from input to output. Since Π-type and bridged Π-type topologies have two shunt switches, they are both better in attenuating capability with respect to T-type and bridged T-type topologies.

5.3 Design of an Individual Attenuator Block

As mentioned earlier, the designed attenuator utilizes switched Π and T type topology. Π-type attenuation blocks are composed of a series NMOS switch and two shunt NMOS switches while T-type consists of one series and one shunt NMOS switch. Figure 39 represents simplified models and signal flow patterns of Π-type in a) reference b) attenuation states and T-type in c) reference d) attenuation states. R_1, R_2 and R_3 resistors are used for both impedance matching and attenuation adjusting purposes. In reference state, series NMOS is turned-on but shunt devices are turned-off while the biases are reversed in attenuation mode.

In order to switch between attenuation and reference states, series and shunt devices must be conversely biased. Hence, inverters are used for providing this condition in all attenuation blocks while decreasing number of pads needed. If PMOS switches are used as series or shunt switch, then, there is no need for using inverters but size of PMOS for the same attenuation level must be approximately three times greater than NMOS, which makes internal capacitances higher. The size of series and shunt transistors directly affects IL, attenuation level and phase variation between reference state and attenuation state. If size of shunt devices increases attenuation capability of the block increases but due to increase in internal capacitors IL also increases.

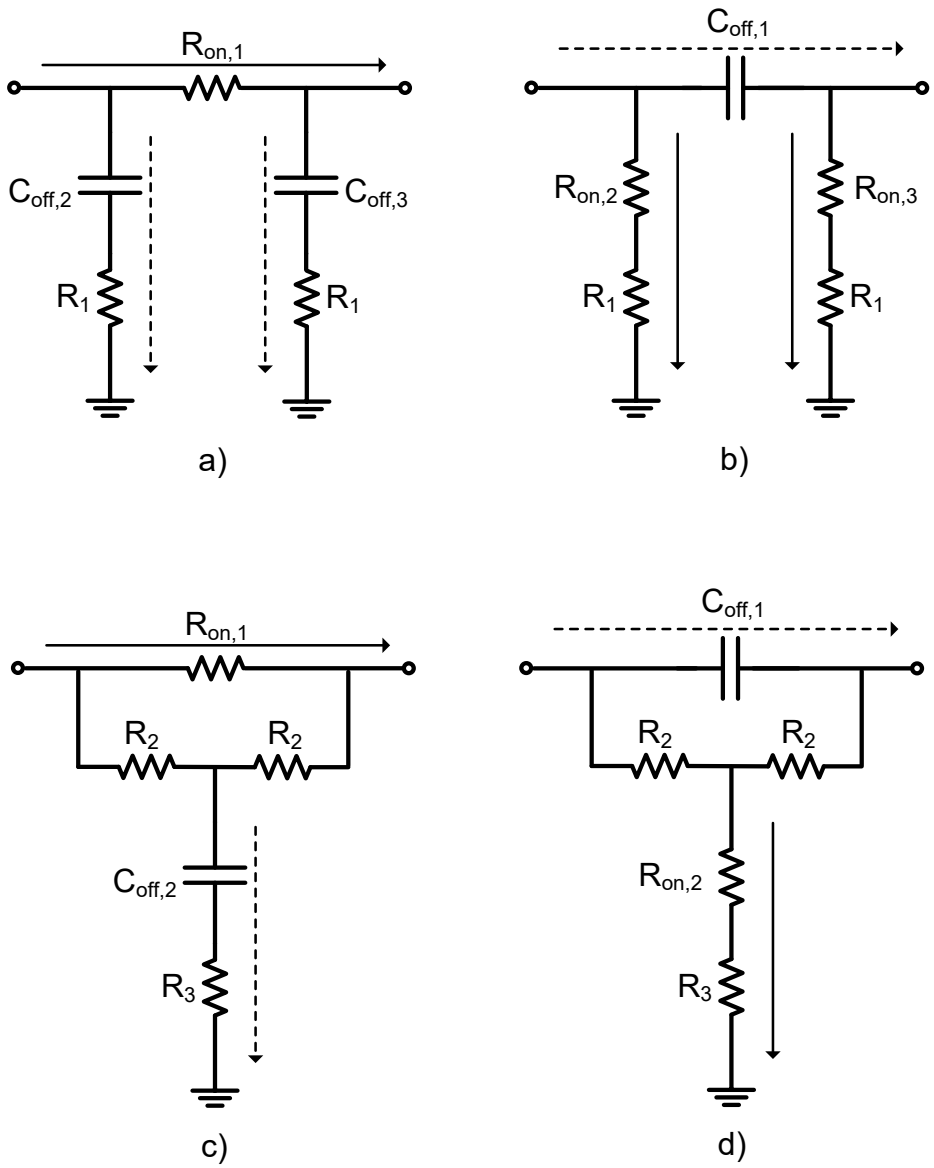

Figure 39: Simplified models and signal flow patterns of Π-type in a) reference b) attenuation states and T-type in c) reference d) attenuation states.

Therefore, the size of shunt NMOS switches must be optimized by taking into account both attenuation and IL specifications. Moreover, the R_{on} and internal capacitances of series NMOS also have significance for IL and attenuation of the block. If the R_{on} resistance of series NMOS is high, IL increases because input signal passes through this R_{on} resistance which is inversely proportional to size of the device.

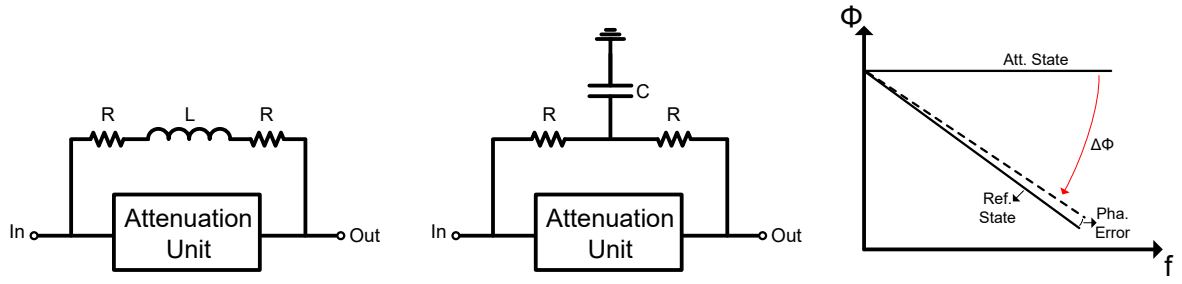

Figure 40: (a) inductive and (b) capacitive phase/amplitude correction networks with their operating principle (c)

5.4 Phase/Amplitude Correction Network

Phase and amplitude errors are significant specifications for an attenuator because along with the phase shifter (PS), they determine phase/amplitude error of the overall T/R module system which is also related to side lobe levels and beam sharpness of the phased array radar system.

As a consequence of series and shunt internal capacitances that can never be reduced to zero, transition phase in between reference and attenuation states varies and this problem is not counteracted with conventional Π-type attenuator topology [62]. Thus, in this design, low pass filters are used for phase/amplitude correction purpose as shown in Figure 40 (a) and (b) [62].

Phase and amplitude errors of the attenuator calculated by root mean square method. RMS error calculation is performed by adding squares of errors inserted by each attenuation state and then dividing total error to number of the states which is 128 in our case due to 7-bit operation.

5.5 A 7-Bit CMOS Step Attenuator with Low Amplitude Error

In this design, combination of cascaded switched Π-type and T-type attenuator blocks are utilized in order to have 7-bit operation. There are 7 attenuation blocks consisting of 4 T-type and 3 Π-type. For higher attenuation blocks (8.32dB, 4.16dB, and 2.08dB) Π-type networks (Fig. 3d) are used because they are more capable of attenuating with respect to T-type topology. For lower attenuation blocks (0.13dB, 0.26dB, 0.52dB, 1.04dB) T-type attenuators are used instead of Π-type for lower IL and better impedance matching. Capacitive and inductive low pass filters are deployed in order to eliminate phase variation between reference and attenuation states.

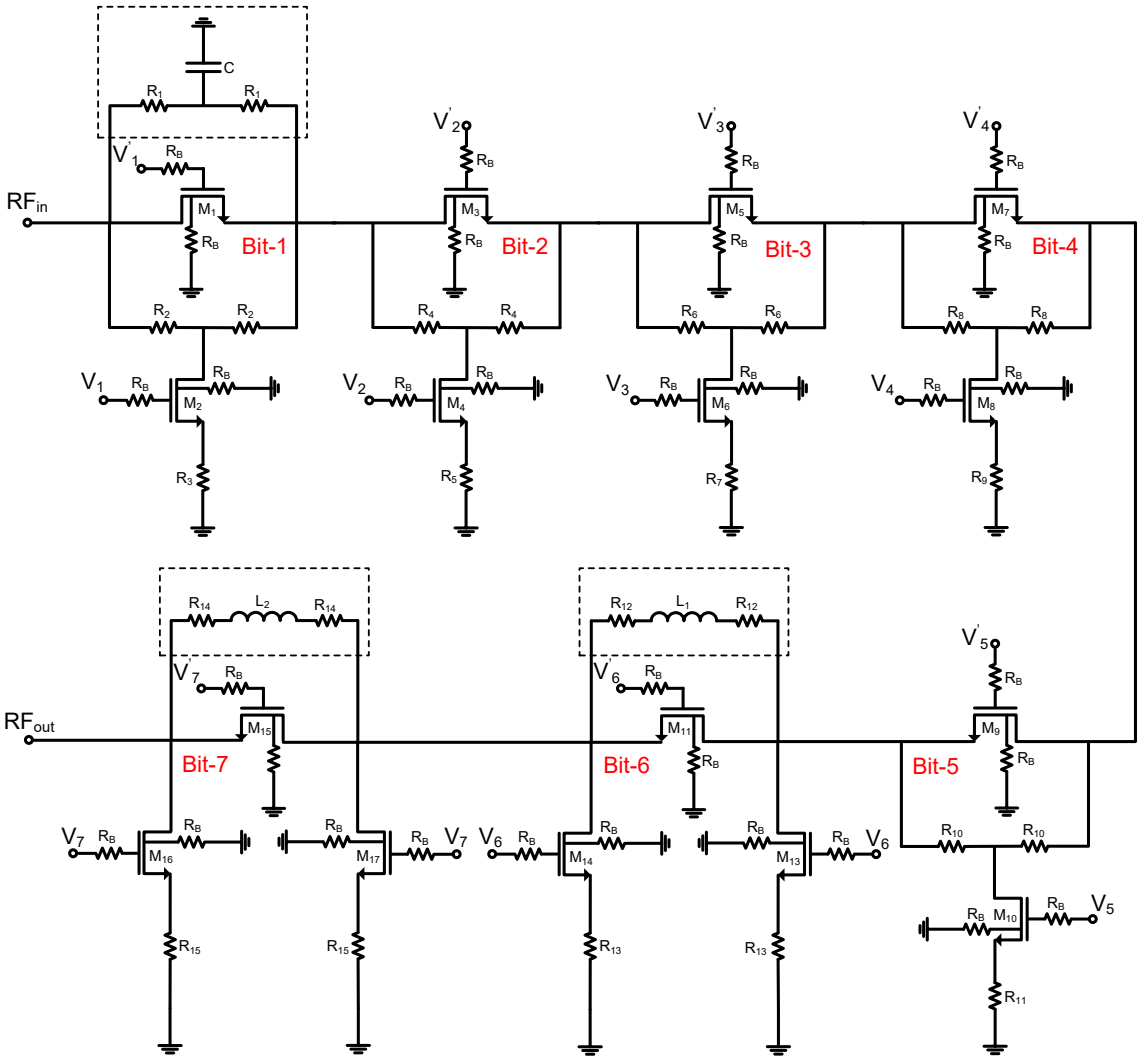

Figure 41: Schematic view of the designed 7-Bit CMOS step attenuator

As the first step, seven attenuation blocks which have relative attenuations of 0.13 dB, 0.26 dB, 0.52 dB, 1.04 dB, 2.08 dB, 4.16 dB and 8.32 dB are designed with phase/amplitude correction networks and matched input and output impedances. Then, the designed individual attenuation blocks are cascaded to each other in the order from lower to higher attenuation block (Figure 41).

The order of attenuation blocks is important for power handling capability of the whole design because lower attenuation blocks are more linear than the higher attenuation blocks. Therefore, lower attenuation blocks are placed at the front end of the attenuator chain because in lossy circuits overall linearity performance is determined by the initial blocks.

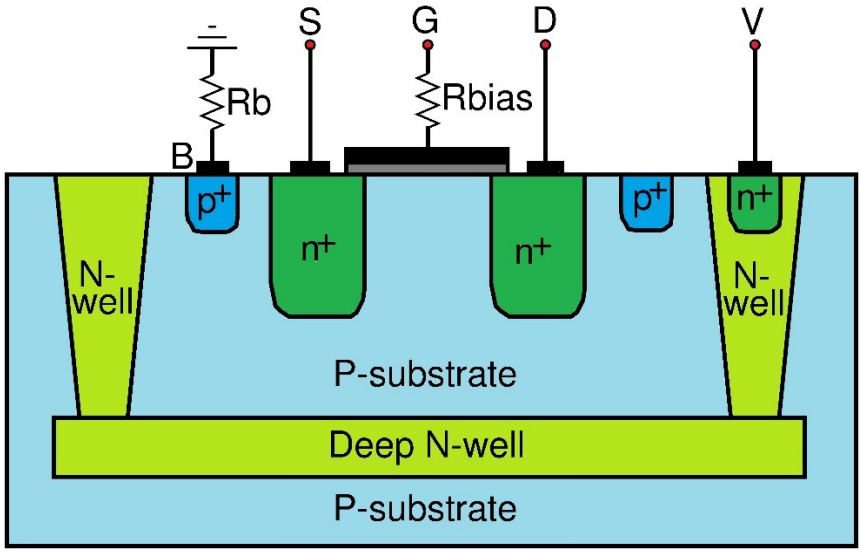

Figure 42: Cross section of an isolated NMOS Transistor

5.6.1 Switch Design via Isolated NMOS

In order to understand operating mechanism of an attenuator block, analysis of internal capacitances of NMOS switches is critical because IL, attenuation and phase error specifications are directly related to variations in those capacitances. In a NMOS switch, the NMOS device only operates in cut-off and triode regions. Gate-to-body (C_{gb}), gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances vary as operating region changes. However, junction capacitances (C_{sb} & C_{db}) are the same for both cut-off and triode modes of operation. As a consequence of variation in internal capacitances of NMOS among cut-off and triode regions, phase and amplitude error occurs in an attenuator block. Figure 43 represents capacitive device model of a NMOS in (a) cut-off and (b) triode mode of operation.

The switch designed via isolated NMOS (Figure 42) has significant advantages such as lower IL and higher linearity over the ones designed by conventional NMOS. Body of the isolated NMOS is separate from main substrate owing to double well process. Isolated NMOS structure allows body of the device to be grounded through a high resistance (R_b). In a NMOS switch, use of R_b results in elimination of shunt drain-to-body (C_{db}), source-to-body (C_{sb}) and C_{gb} capacitances. Consequently, leakage current through these capacitors is removed.

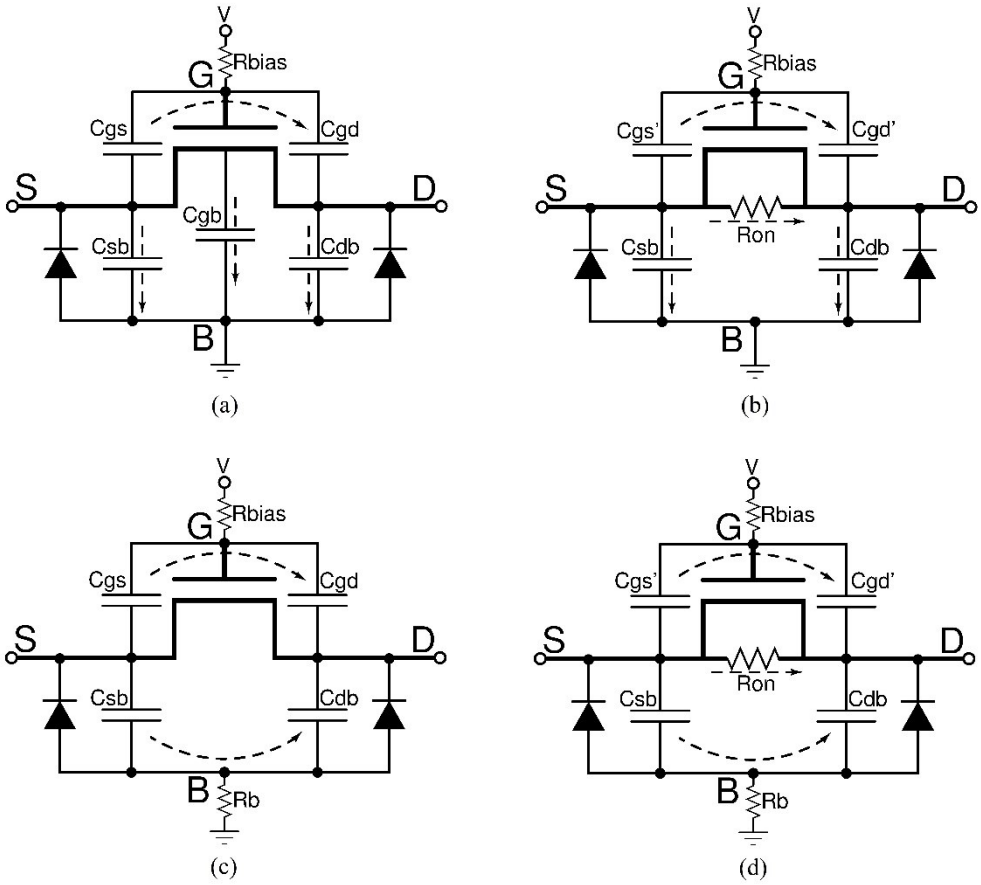

Figure 43: Capacitive models for conventional (a) turned-off switch (b) turned-on switch and (c) turned-off switch with isolated NMOS (d) turned-on switch with isolated NMOS

Moreover a large R_{bias} resistor is used in order to prevent signal leakage through gate capacitance towards bias voltage source which is AC ground. Figure 43 represents signal flow path in a NMOS switch designed using conventional NMOS and isolated NMOS devices. Figure 43 (a) and (b) represents a conventional NMOS switch states whereas (c) & (d) shows isolated NMOS switch states. As seen from Figure 43 (a), RF signal is flowing to ground through C_{sb}, C_{db} and C_{gb} capacitors. On the other hand, in Figure 43 (c) R_b resistor prevents this undesired signal loss while eliminating C_{gb} capacitor.

In the switched-off state configuration represented in Figure 43 (c), no signal flows through C_{gb} due to fact that two ports of this capacitor are biased to the same voltage because of equivalence of C_{gs} to C_{gd} and C_{sb} to C_{db} (acts as a wheatstone bridge). Hence, the IL caused by signal flow through C_{gb} capacitor is avoided in contrast to the case shown in Figure 43 (a).

Figure 43 (b) and (d) demonstrates signal flow paths when the switches are in on-state where NMOS transistors operate in triode region. As seen from Figure 43 (b), there is signal loss through junction capacitances C_{sb} and C_{db}. However as seen in Figure 43 (d) entire RF signal is conducted as R_b prevents signal flow towards ground resulting in IL. Therefore using isolated NMOS has an advantage over conventional NMOS structure in terms of IL performance. If switch is used only to provide drain-to-source isolation, utilizing isolated NMOS degrades performance because in cut-off region there would be an additional path ($(jwC_{sb}+jwC_{db})/2$) for signal flow from drain to source. On the other hand, if the switch is designed for building an attenuator block in which relative difference between turn-on and turn-off states is important, iNMOS is much better in performance than conventional NMOS structure because switching operation is directly provided from input to output without any considerable effect of shunt parasitic capacitances.

5.6.2 Advantages of Utilizing INMOS for Attenuator Design

In this attenuator design isolated NMOS is employed in order to achieve low IL. If NMOS switch models in Figure 43 are substituted into Π-type attenuator topology in Figure 38 (a), capacitive model for an attenuator block in reference state can be depicted as in Figure 44. R_3 resistors are used for compensating decrease in attenuation and providing better impedance matching. In Fig. 4, series and shunt Y-parameters for Π-type attenuator designed via conventional NMOS (Y_1, Y_2 & Y_3) (a) and isolated NMOS (Y_1', Y_2', Y_3') (b) are used for calculating S_{21} and S_{21}' while the attenuator block is in reference state.

$$Y_1 = Y_2 = \frac{j\omega C_{gd} - \omega^2 R_1 C_{gd} C_{db}}{2 + j\omega R_1 (2C_{db} + C_{gd})} + 2j\omega C_{db} \tag{26}$$

$$Y_1^{'} = Y_2^{'} = \frac{j\omega (C_{gd} + C_{db})}{2 + j\omega R_1 (C_{db} + C_{gd})} \tag{27}$$

$$Y_3 = \frac{R_2 + R_{on}}{R_2 R_{on}} + \frac{j\omega C'_{\mathrm{gd}}}{2} \tag{28}$$

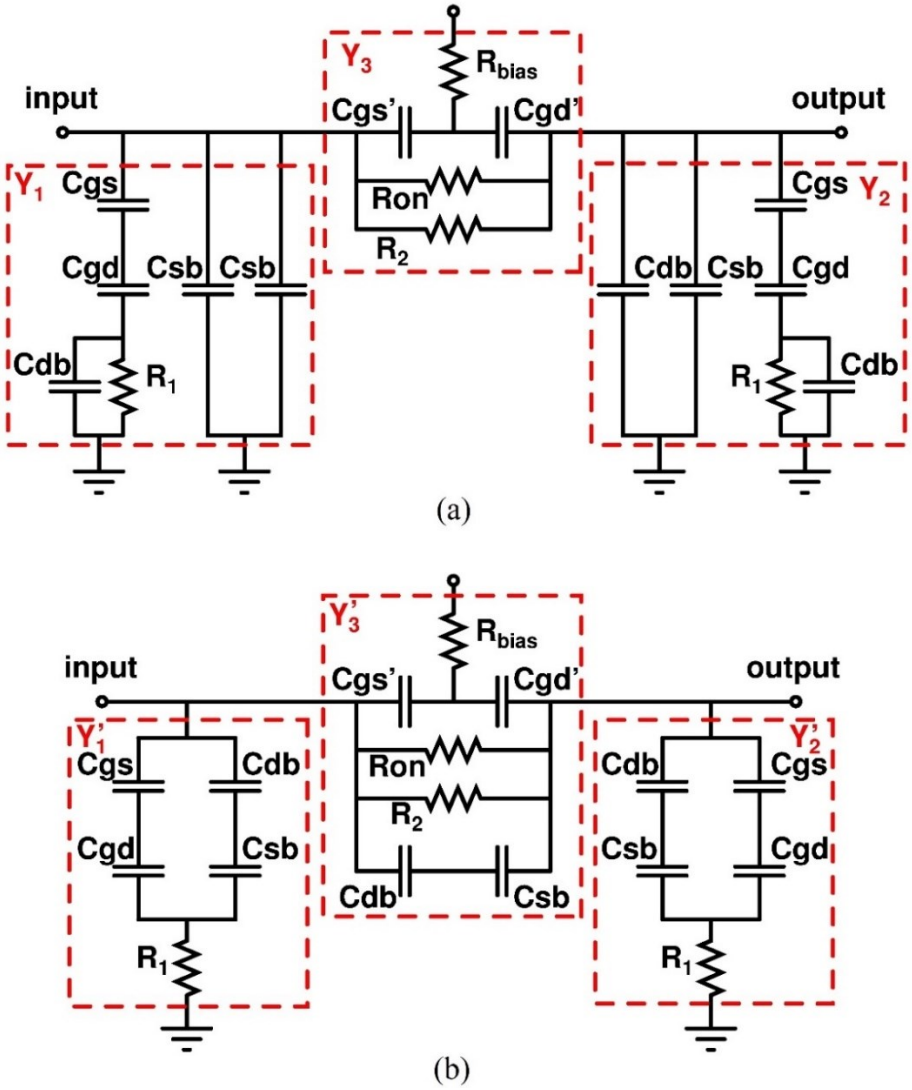

Figure 44: Capacitive model for Π-type attenuator designed with (a) NMOS (b) Isolated NMOS

$$Y_3^{'} = \frac{R_2 + R_{on}}{R_2 R_{on}} + \frac{j\omega C'_{\mathrm{gd}}}{2} + \frac{j\omega C_{db}}{2} \tag{29}$$

For Π-type admittance network ABCD parameters are calculated as followed:

$$A = 1 + \frac{Y_2}{Y_3} \qquad B = \frac{1}{Y_3} \qquad C = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3} \qquad D = 1 + \frac{Y_1}{Y_3} \tag{30}$$

By using ABCD-parameters S_{21} and S_{21}' are calculated via following equation:

$$S_{21} = \frac{2}{A + B / Z_0 + CZ_0 + D} \tag{31}$$

As seen from the equations (26) and (27), Y_1 and Y_2 are greater than Y_1' and Y_2' because second term of (26) is the dominating term. In addition Y_3' is larger than Y_3 because it has additional admittance contributed by C_J. S_{21} (IL) of a Π-type attenuator implemented with NMOS can be calculated by substituting equations (26) and (28) into (31). If the attenuator is designed using isolated NMOS S_{21}' can be calculated by substituting equations (27) and (29) into (31). As seen from the equation (31), for the case in which the attenuator is designed by using isolated NMOS, A', B', C' and D' parameters are all greater than the parameters of the one designed with conventional devices. As a result, S_{21}' of the attenuator designed via isolated NMOS is greater than an attenuator designed via conventional NMOS ($S_{21}'>S_{21}$). Therefore, it is concluded that isolated NMOS in Π-type attenuator design decreases IL.

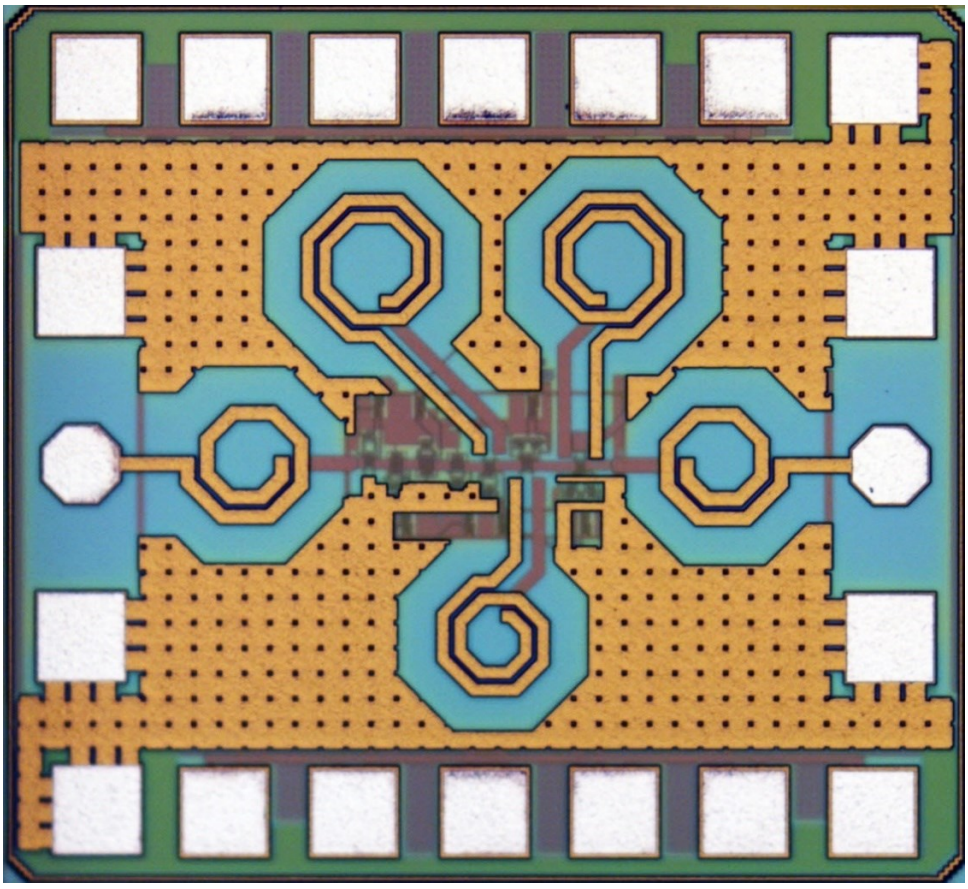

Figure 45: Die snapshot of the implemented 7-Bit CMOS Step Attenuator

5.6.3 Measurement Results

The designed attenuator is measured with the help of using test bench explained in Appendix A. Figure 45 illustrates die snapshot of the attenuator. Layout is implemented by using Cadence while electromagnetic simulations are performed with SONNET. The die occupies (0.76x0.83) 0.63 mm^2 including pads. DC biases are applied by programing power supplies with the help of LAB View due to high number (128) of attenuation states. Following the extraction of S-parameters for each state RMS amplitude and phase errors are calculated.

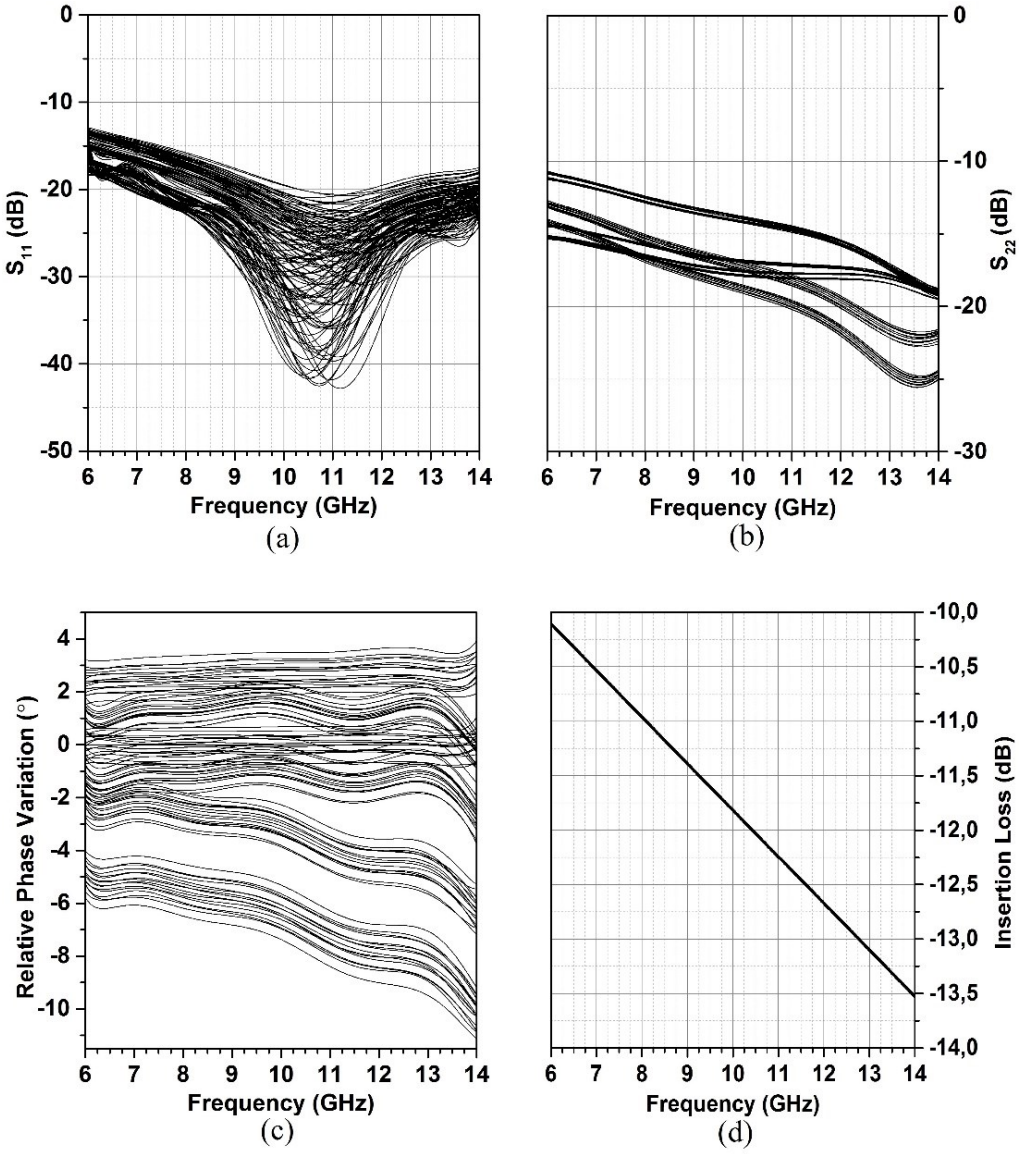

Figure 46: Measured (a) S_{11} (b) S_{22} (c) Relative Phase Variation (d) IL

Figure 46 represents measured S_{11} (a), S_{22} (b), relative phase variation (c) and IL (d) of the attenuator. As seen from the graphs (a) and (b), measured input and output impedance of the attenuator are well-matched to 50Ω across 6-14 GHz frequency band. IL is S_{21} of the attenuator while all the blocks are at reference state. As seen from Figure 46 (d) measured attenuator has almost the same IL with similar works in the open literature despite it has more bits. Figure 46 (a) demonstrates measured attenuation states extending to 16.51 dB with the increments of 0.13dB between successive states. As seen from the graph, designed 7-bit CMOS step attenuator is capable of adjusting signal power with high resolution and precision while providing low variation in the phase. Figure 46 (b) represents measured RMS phase and amplitude error of the attenuator. As seen from the graph this attenuator operates as 7-bit between frequencies of 7.75 GHz and

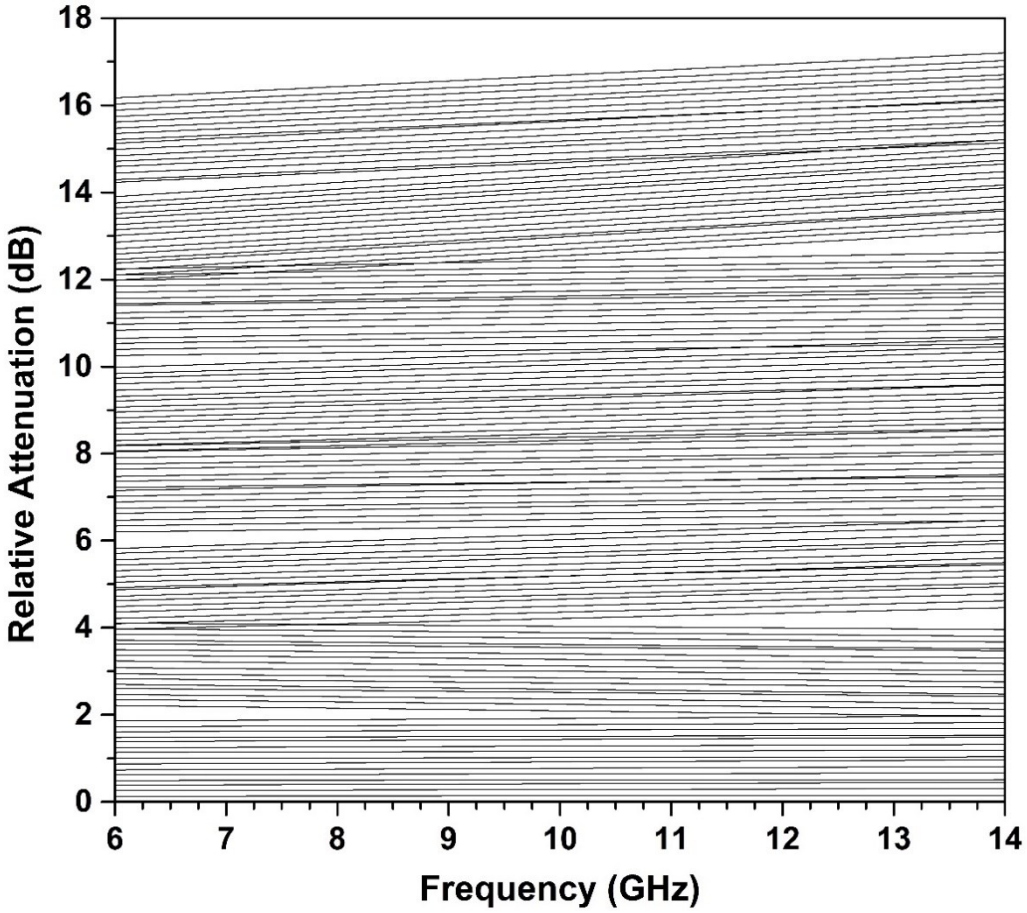

Figure 47: Measured (a) Relative Attenuation Steps (b) RMS Phase (right) and Amplitude Error (left)

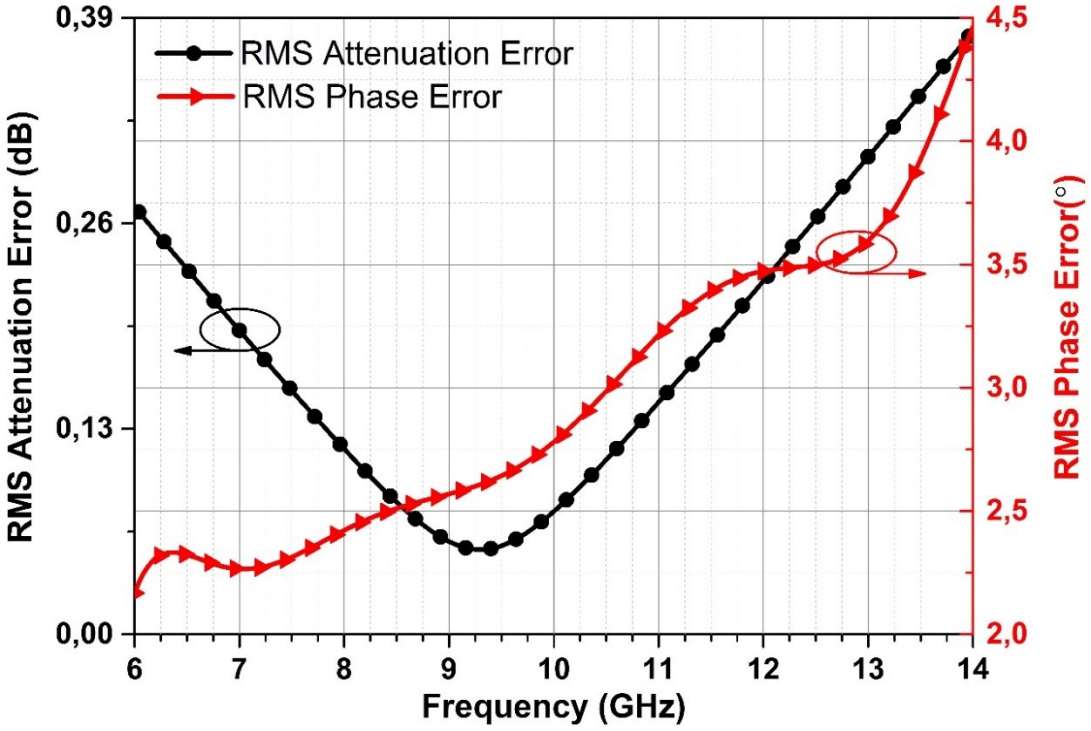

Figure 48: Measured RMS attenuation error and Phase Error of the CMOS attenuator

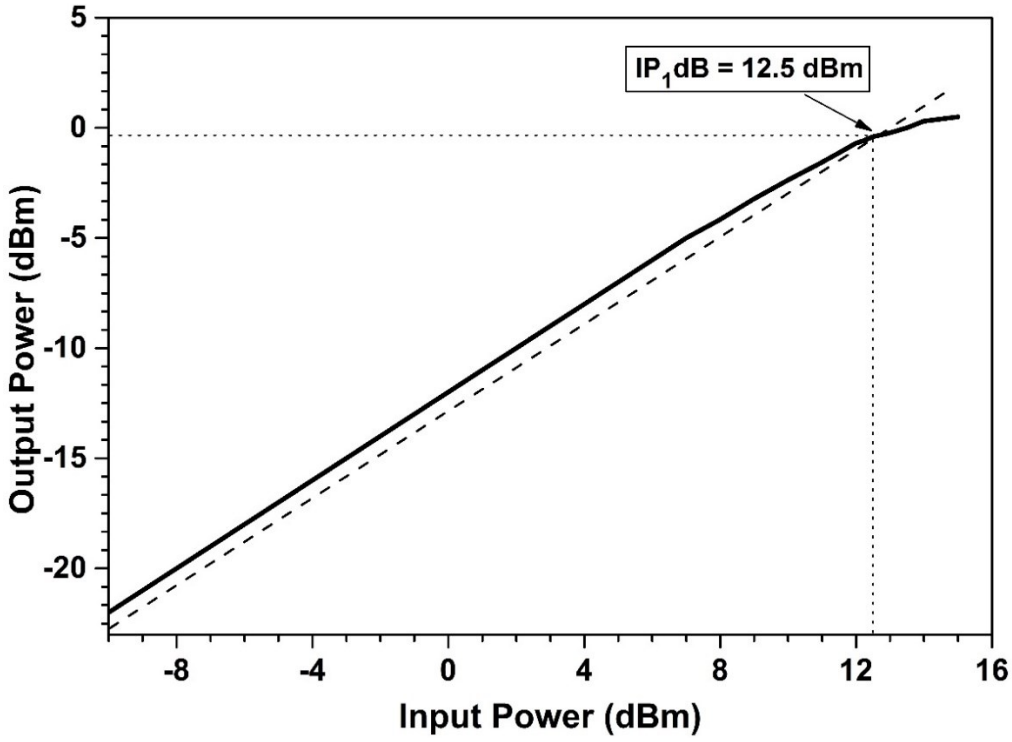

Figure 49: Measured P_{1dB} of the CMOS attenuator

10.75 GHz at which RMS attenuation error is lower than the attenuation level of least significant bit (0.13dB). In addition, it can operate as 6-bit in a wideband of frequencies which is from 6 GHz to 12.5 GHz. In 7-bit operation, highest value of the RMS phase error is 3.1° whereas in 6-bit of operation 3.5°. Fig. 8 represents measured 1-dB compression of the attenuator. According to the graph measured input referred 1-dB compression point of the attenuator is 12.5 dBm at 10 GHz besides output referred P_{1dB} is -0.5 dBm. This attenuator operates in relatively low attenuation range but it possesses capability of adjusting the attenuation level with the increment of 0.13 dB. Low attenuation increment results in more accurate amplitude setting for the system. Moreover, this is the foremost 7-bit step attenuator designed for X-band phased array radar applications among the similar work available in the open literature.

5.6 7-Bit SiGe BiCMOS HBT Digital Step Attenuator

The previously designed 7-Bit CMOS step attenuator performs well in terms of resolution, phase/amplitude error and power handling capability. However, due to the high parasitic C_{off} capacitances of the CMOS devices, it exhibits a relatively high IL. In addition, attenuation range of 16.51 dB is also relatively high with respect to the similar work in the open literature. Therefore, an alternative solution for switching operation in the attenuator is required. Eventually, a 7-bit attenuator utilizing HBTs instead of MOS based transistors as switch is designed and implemented in IHPH3 0.25µm SiGe BiCMOS technology.

5.6.1 Circuit Design and Analysis

In this section, design and implementation of a 7-bit digitally controlled HBT step attenuator is presented. The designed HBT attenuator has the same circuit configuration as previously designed CMOS attenuator. Furthermore, the same phase/amplitude correction networks are also employed in the design of HBT attenuator. As mentioned above, this attenuator consists of HBT switches oriented in Π/T type topology.

In order to improve IL performance, the reverse saturation technique which is previously explained in section “4.3.2 Reverse Saturation” is employed. Therefore, lower IL values in X-band are achieved with respect to CMOS attenuator. Moreover, HBT attenuator covers attenuation range

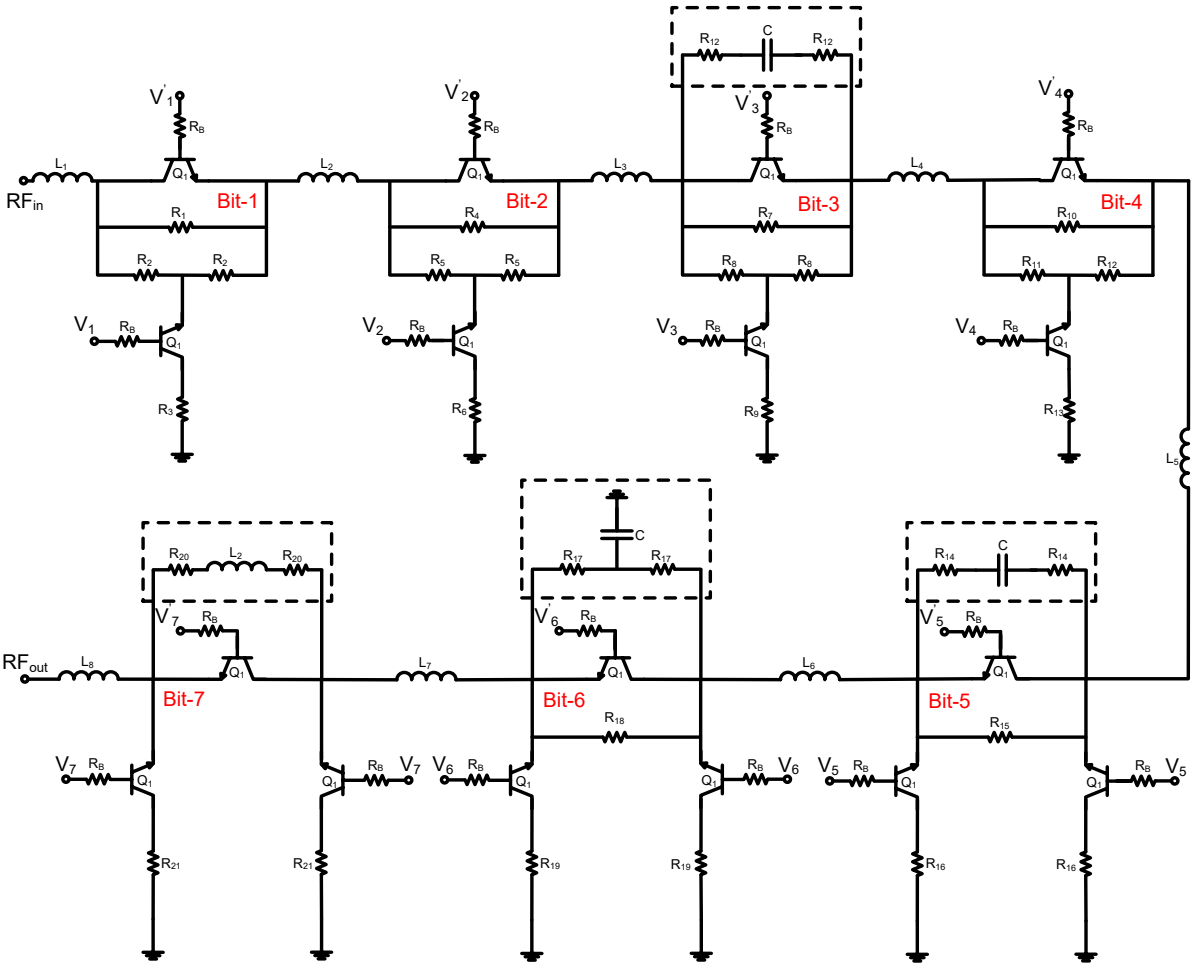

Figure 50: Schematic circuit configuration of the designed 7-Bit SiGe HBT Attenuator

of 31.5 dB with the increments of 0.25dB which is approximately two times higher than CMOS attenuator. Power handling capability of the HBT attenuator is also higher than the CMOS attenuator. The detailed analysis on SiGe HBT switches has been done in section 3.3.1. The designed attenuator possesses all inherent advantages of utilizing HBTs at the cost of additional DC power consumption and area occupation.

5.6.1 Post-Layout Simulation Results

Layout of the designed 7-bit SiGe HBT attenuator is done in cadence environment whereas EM simulations for inductors and interconnection lines are performed on SONNET for precise modeling. Figure 51 represents snapshot of the layout which occupies an area of 0.96 mm^2 (1.27mm x 0.76mm) including pads. As seen on the layout, there are too many inductors which

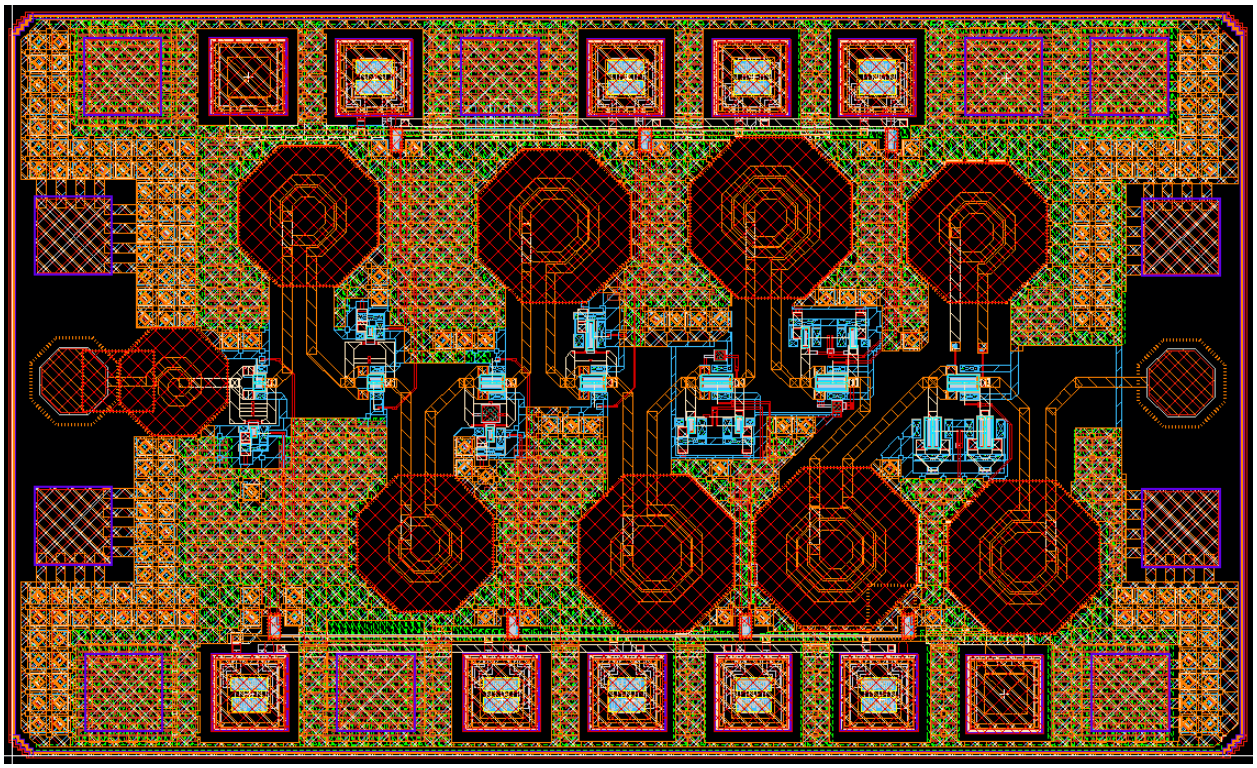

Figure 51: Layout of the designed 7-Bit SiGe HBT Attenuator

may electromagnetically couple with each other and distort aimed performance characteristics. Hence, all the inductors are simultaneously simulated via SONNET in order to take mutual inductance effect into consideration. Inverters are designed and implemented to decrease the number of required bias pads for switching each attenuation block. In order to prevent ESD to damage gate of the MOS devices employed in the inverter, two back-to-back diodes are connected to each bias pad.

The simulations are run on the complete layout version of the attenuator where RC parasitic effects are included as well as magnetic coupling among the inductors. Figure 52 represents the simulated S_{11}, S_{22}, IL and relative phase variations of the HBT attenuator for each attenuation state. As seen in Figure 52 (a) and (b), the designed attenuator exhibits a high and wideband RL performance covering more than the frequency range of 6-14 GHz for all 128 attenuation states. As a result of varying C_{off} and R_{on} values, RL also changes depending on the amount of attenuation. In addition to RLs, transmission phase inserted by the attenuator is also deviates depending on different attenuation states.

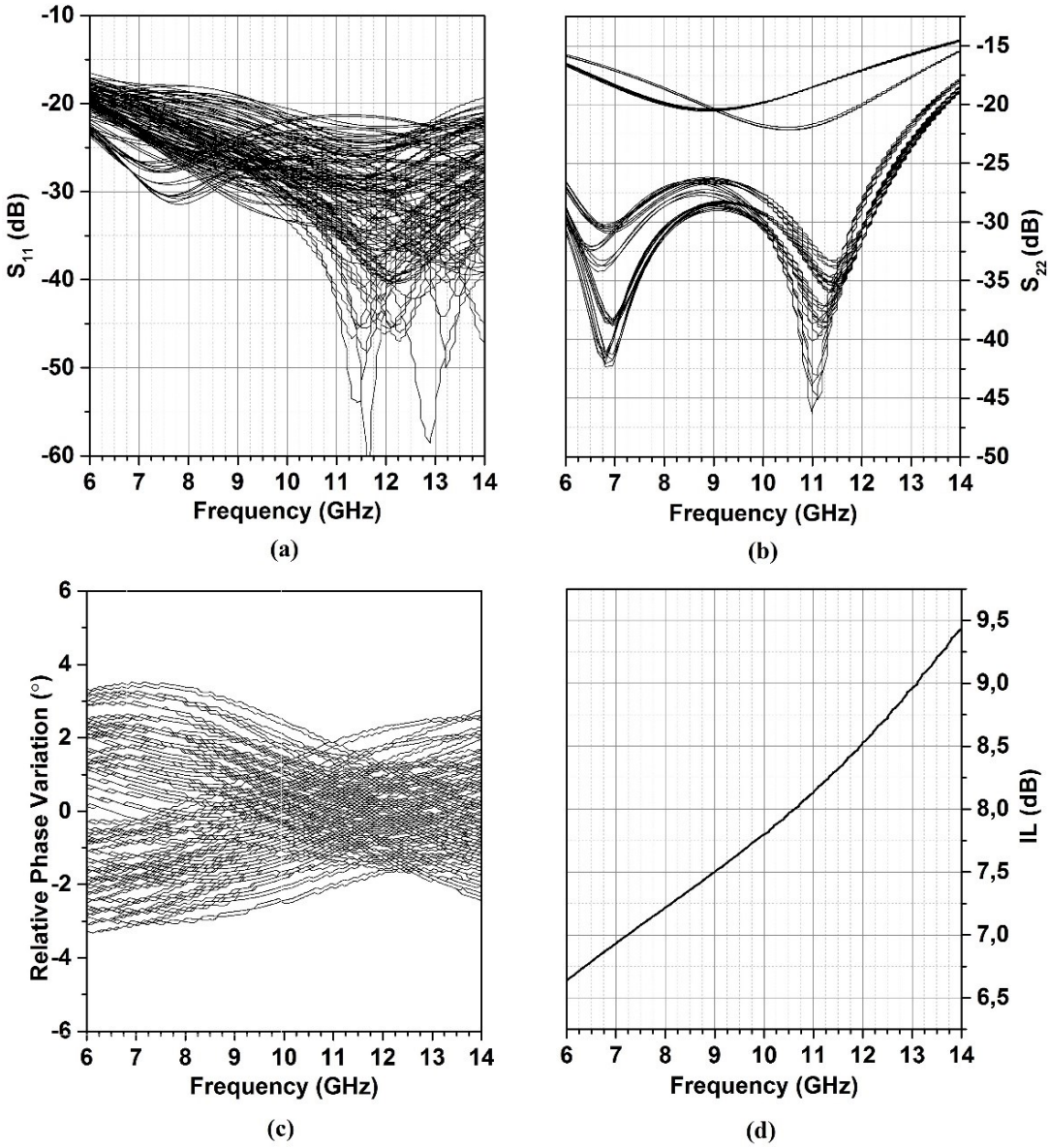

Figure 52: The simulated (a) S_{11} (b) S_{22} (c) Relative Phase Variation (d) IL

Figure 52 (c) illustrates relative variation of the insertion phase which is undesired for the system level performance. Moreover, the simulated IL of the attenuator is shown in Figure 52. As seen on the graph, for X-Band the HBT attenuator exhibits an IL of at most 8.5dB which is much lower with respect to the previously designed CMOS attenuator.

Figure 53 illustrates relative attenuation states covering the attenuation range of 31.5 dB, which is higher than range of the previously presented 7-bit CMOS attenuator.

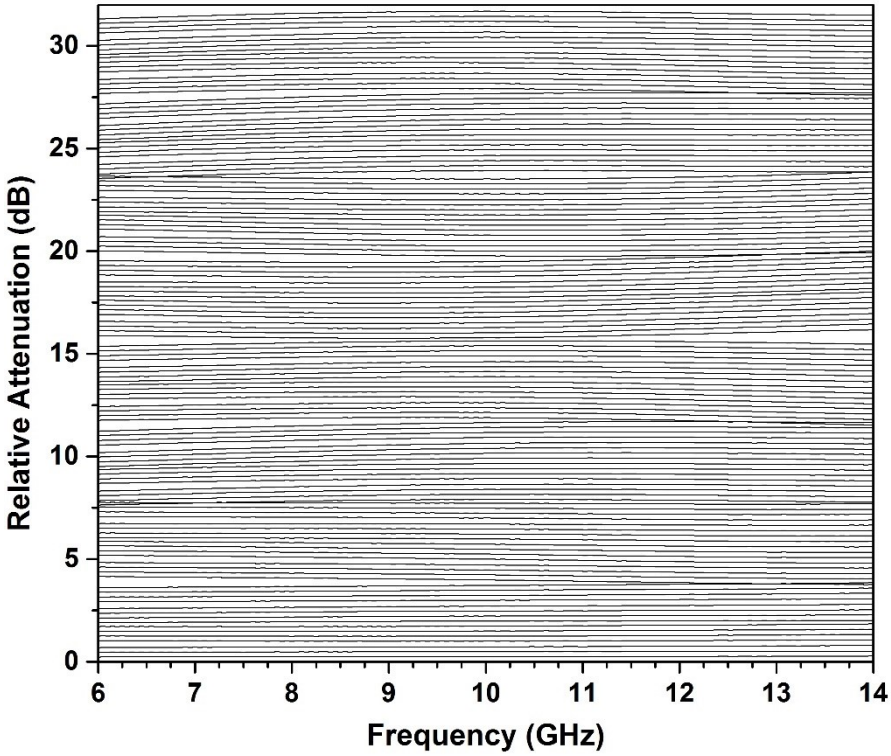

Figure 53: Simulated relative attenuation steps of the HBT attenuator

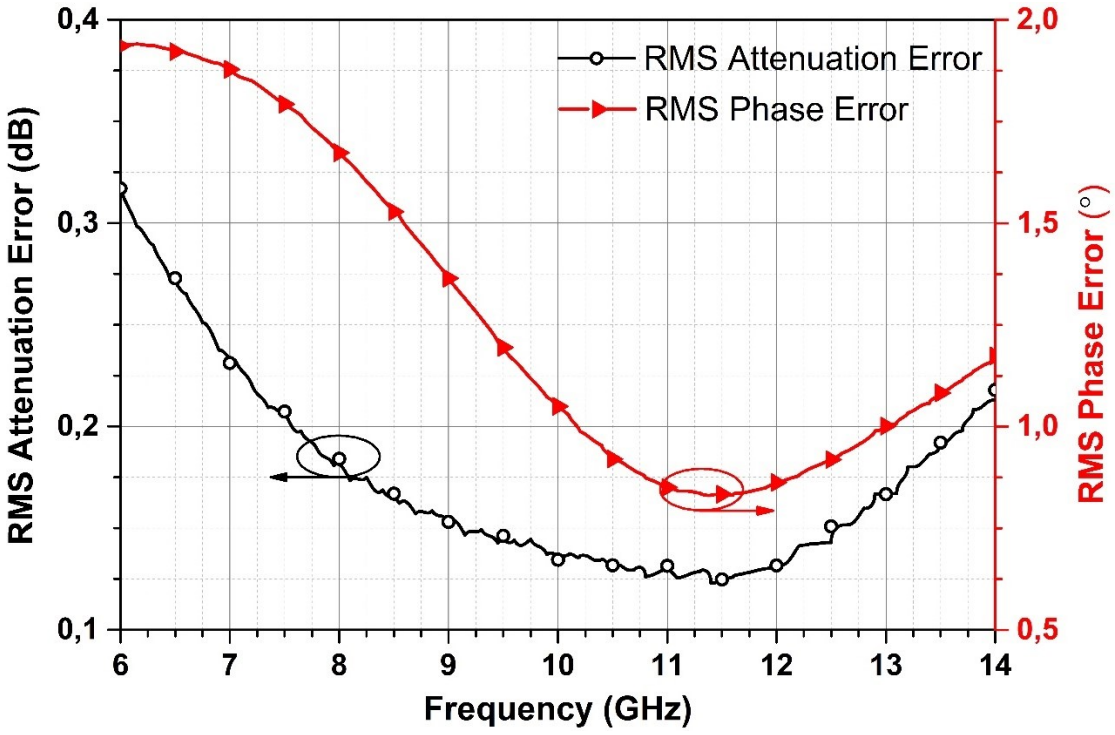

Figure 54: Simulated RMS attenuation error and Phase Error of the HBT attenuator

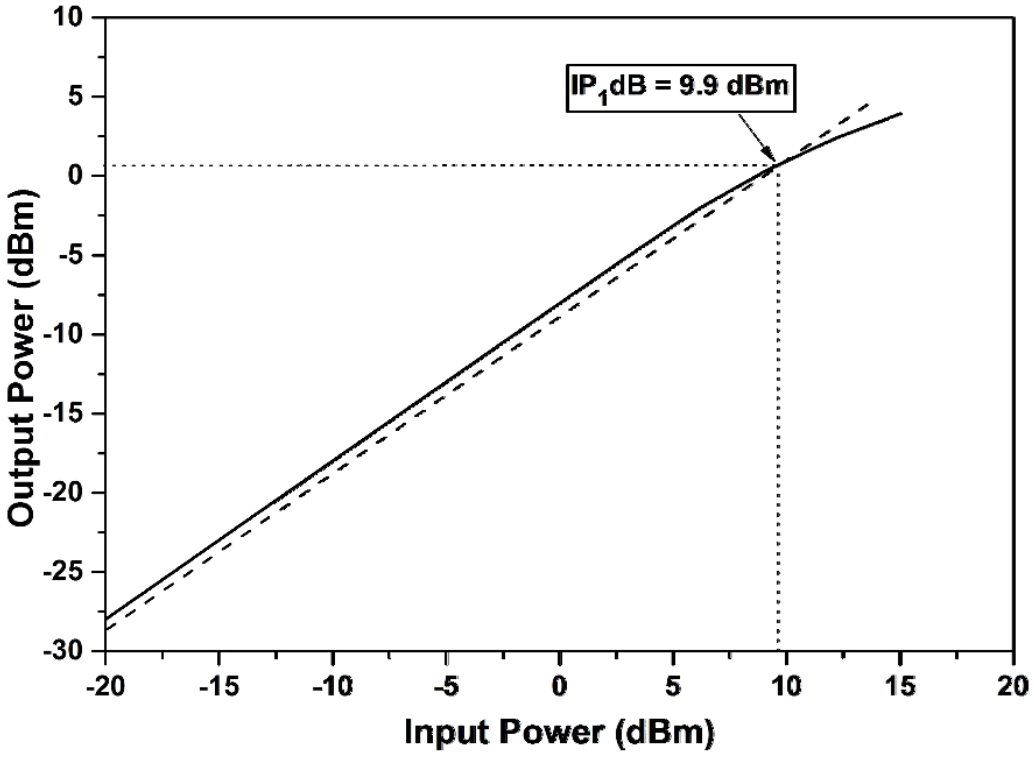

Figure 55: Simulated post-layout P1dB of the designed 7-bit HBT attenuator

As seen on the graph, the attenuation states are almost equally spaced from each other and parallel across a wide frequency band of 6-to-14 GHz which results in low RMS attenuation error as depicted in Figure 54. The graph represents that the RMS amplitude error of the attenuator is lower than the LSB (0.25 dB) in a wide frequency range. In addition, Figure 54 represents the RMS phase error inserted by the attenuator to the system. RMS phase error is at most 1.7 ° across X-band which is a sufficient performance for the designed T/R module to operate in 7-bit resolution.

5.7 Benchmarking

This section represents performance comparison of the designed 7-bit CMOS high precision step attenuator with low amplitude error and 7-bit SiGe BiCMOS HBT digital step attenuator with respect to similar work in the open literature. Table IV shows performance parameters of the designed 7-Bit step attenuators along with earlier reported work available in the open literature.

Table IV: Performance Comparison of the 7-Bit Step Attenuators with Similar Work Available in Open Literature

Ref.	**Freq. (GHz)**	**Tech.**	**# of Bits**	**Att. Range (dB)**	**LSB (dB)**	**IL (dB)**	**RL (dB)**	**P_{1dB} (dBm)**	**RMS Att. Err. (dB)**	**RMS Pha. Err. (°)**	**Die Area (mm^2)**
[62]	8-12	0.18µm CMOS	6	31.5	0.5	<11.3	>11	13	<0.4	<2.2	0.34*
[63]	8-15	GaAs	6	23.5	0.5	<4.5	>8	N/A	<0.45	N/A	6
[64]	DC-20	GaAs	4	23.5	1.5	<5	>13	24	0.5	N/A	4.16
[65]	DC-18	GaAs	5	27.9	0.9	<7	>17	24	<0.5	10	3.84
[66]	10-67	0.18um BiCMOS	4	32 -43	3	<15.2	>8.7	13	N/A	N/A	0.77
[61]	10-50	0.12um BiCMOS	5	23	1	2-3	>8	5	N/A	<3	0.15*
HBT Att.	**7.5-13.5**	**0.25µm BiCMOS**	**7**	**31.5**	**0.25**	**<8.5**	**>17**		**<0.2**	**<1.8**	**0.97**
CMOS Att.	**7.75-10.75**	**0.25µm BiCMOS**	**7**	**16.51**	**0.13**	**<12**	**>15**	**12.5**	**<0.13**	**2.3-3.1**	**0.63**
	6-12.5		**6**			**<12.7**	**>13**		**<0.25**	**2.2-3.5**	

6. Conclusion & Future Work

6.1 Summary of Work

The T/R modules in next generation phased array radar systems, need to have light weight, high performance, high yield, small size and low cost, in order to allow realization of highly integrated IC solutions especially for commercial applications. In the past, T/R modules had been implemented via III-V based IC technologies, however, due to recent advances in SiGe BiCMOS technology, to develop fully integrated and cost effective T/R modules is possible.

In this thesis, an X-Band 7-Bit T/R module with high precision phase/amplitude control is presented along with a detailed discussion regarding internal blocks such as LNA, SPDT switch, an additional high P_{1dB} LNA used as inter-stage amplifier and a 7-Bit attenuator. All the blocks are implemented in IHP 0.25µ SiGe BiCMOS technology. First of all, individual blocks are designed, implemented and measured one by one after extensive open literature survey had been performed. Subsequently, design mistakes and performance insufficiencies are corrected. Eventually, required performance requirements are met which is followed by combining the blocks in order to realize a fully integrated T/R module. The designed T/R module has a gain of 38dB, RMS random amplitude error of 0.82dB, RMS random phase error of 2.6°, NF of 3dB and RX-TX isolation of 80 dB across X-Band.

Two high dynamic range LNAs are implemented by using inductively degenerated cascode topologies. One of them is single stage cascode LNA while the other one employs two cascaded cascode stages for providing low NF, high gain and linearity, simultaneously. The 1-stage LNA is used as interstage linear amplifier where the 2-stage LNA is employed as an LNA in the T/R module. Moreover, a SiGe HBT SPDT switch with reverse saturation method to improve IL performance, is designed and implemented to be used in T/R module. In addition, a 7-Bit SiGe HBT Π/T type digitally controlled step attenuator is realized in order to provide 7-bit operation T/R module. The designed attenuator includes capacitive and inductive phase error correction networks to decrease RMS phase error of the system. In addition, its capability to adjust amplitude in small increments provides particular advantages to phased array radar systems.

6.2 Future Work

One of the frequently faced problems in this T/R module design is high NF of the LNAs in measurement. Generally, high NF may be caused by a design, measurement or modelling error. One of the solutions to counteract this problem is matching the simulation results to the measurement results by manually adding some parasitic to the circuit. As the following work, these parasitic can be included into the LNA architecture and a new design can be done. Another solution can be decreasing the linearity requirement of the LNA as matter of fact, obtaining high power handling and low NF simultaneously, requires more complex design challenges, which cause deflection from modelled device characteristics.

In addition, relatively high IL of the attenuator can be reduced by utilizing different transistors or adding new techniques to improve performance. In addition, for the purpose of increasing their power handling capability, stacked shunt transistors may be utilized. Another solution can be employing high breakdown voltage HBTs at the cost of reduction in isolation and increase in power dissipation. Moreover, chip area of the attenuator can also be decreased by eliminating usage of too many inductors.

Lastly, after the measurements of the designed T/R modules some of the blocks may require design optimization for achieving better performance parameters. This kind of optimization and modifications on the T/R module are also included in long term future work.

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Appendix A

A) Measurement Setup

This section presents measurement setup that is utilized for measuring all the chips explained in this thesis.

During the measurement procedure of the dies, firstly, FR4 boards are custom designed according to number of bias pads and their location on the design. Afterwards, the dies are pasted on the board by using epoxy which is an electrically conductive glue. Then, all DC pads are connected to the lines created for them on the board, by wire bonding. In order to decrease parasitic effects caused by metal lines or bond wires, DC shunt capacitors in different sizes are soldered. As the next step, device calibrations are performed and DC bias voltages are applied to the die.

Figure 56 represents one of the boards that is fabricated for measuring a microchip.

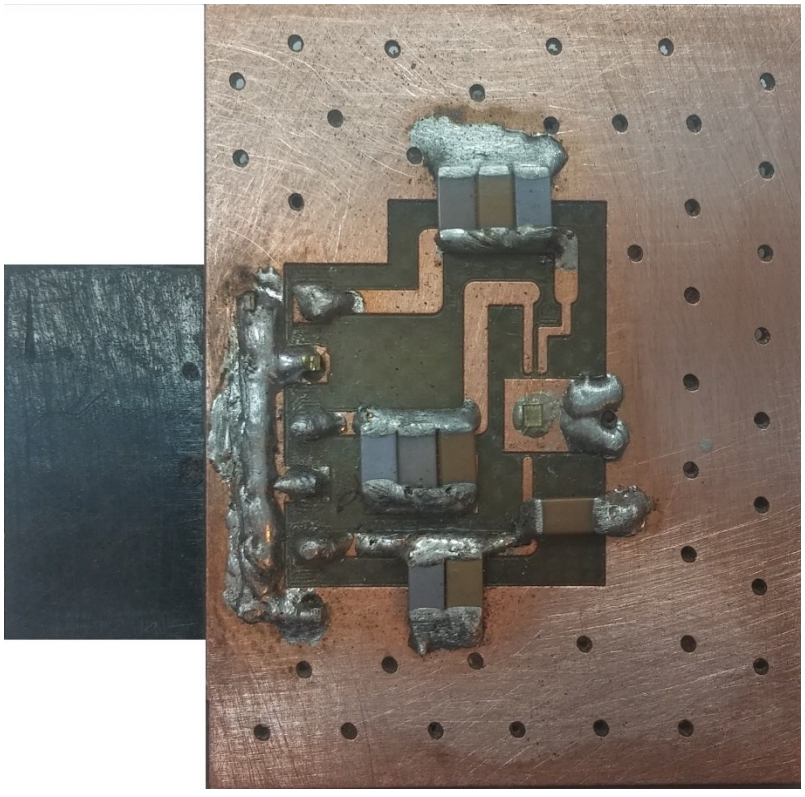

Figure 56: One of the boards that is implemented for measuring a microchip

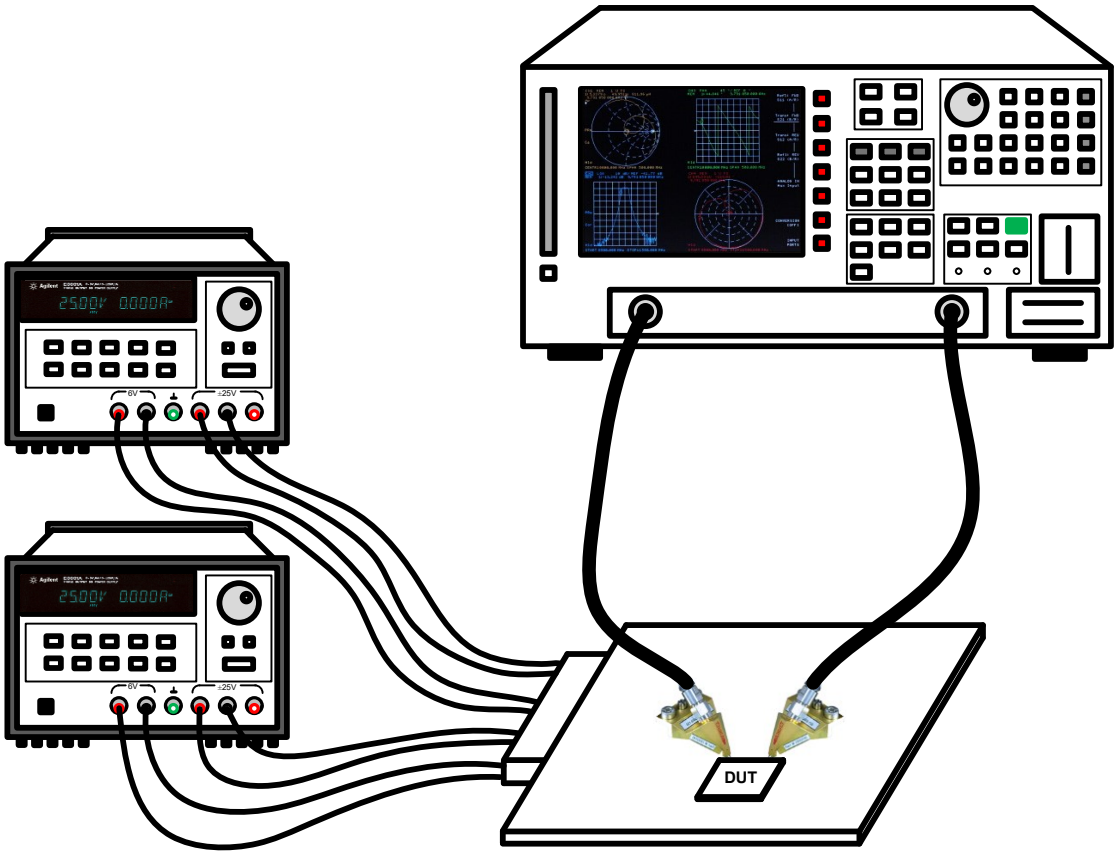

Figure 57: Simplified measurement setup diagram utilized during the measurement of S-parameters

1. S-Parameters Measurement

For all the chips demonstrated in this thesis, the scattering parameters are measured by using Agilent 20 GHz 8720ES two-port network analyzer while the DC bias voltages are applied by Agilent E3631A DC power supply. The employed 50Ω RF probes can be used in measurement across the frequency band of DC-to-40 GHz and their model is Z 040 K3N GSG 150 provided by Z-Probe. The S-parameters measurement procedure is performed by following the steps below:

1) Perform the full two-port calibration of the network analyzer by using the Impedance Standard Substrate (ISS) model of 101-190C provided by Cascade Microtech company.
2) The board taped on our test bench and DC bias voltages are applied.
3) As the last step, RF probes are connected to RF pads and measurement results are exported in .csv file format.

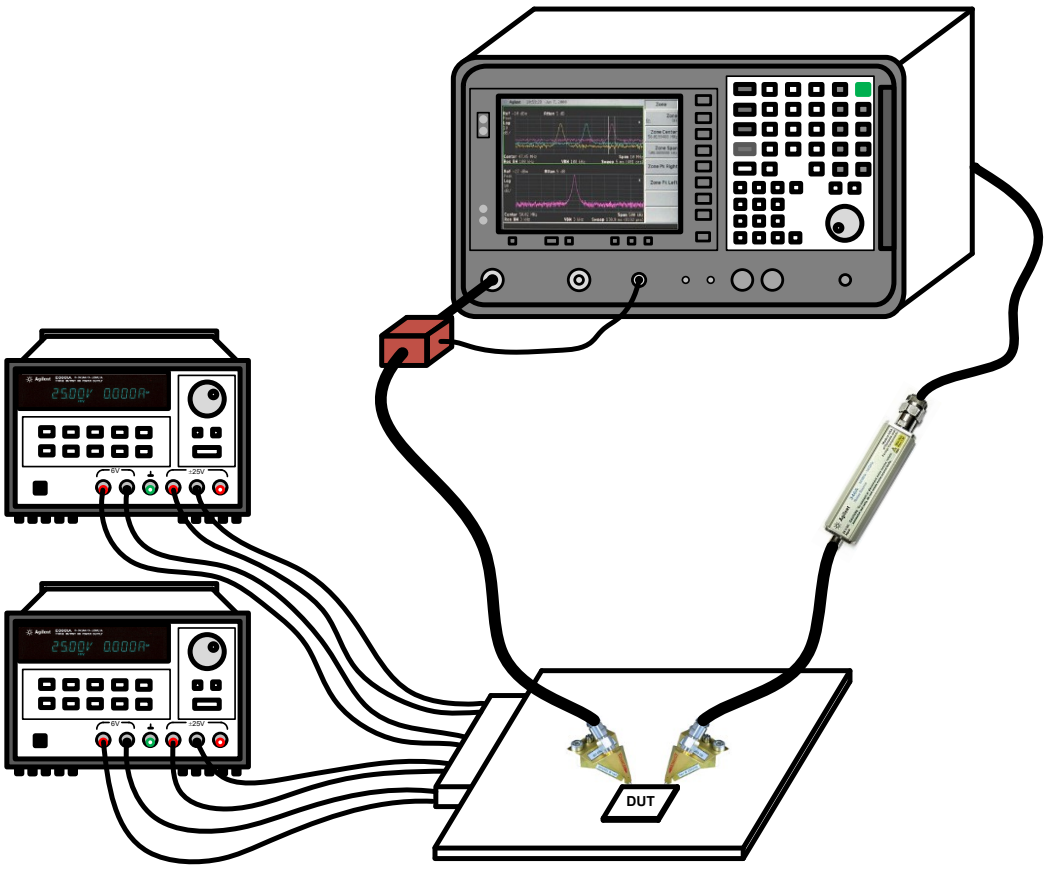

Figure 58: NF measurement setup for the LNAs shown in this thesis

2. Noise Measurement

The NF of the dies represented in this thesis is measured by using Agilent E4407B Spectrum Analyzer. Figure 58 shows measurement setup that we use for measuring the NF. As seen on the diagram, DUT is biased with Agilent E3631A DC power supply and by using Z-probe Z 040 K3N GSG 150 probes, the die connected to the spectrum analyzer. At the input side Agilent 346A noise source is placed. After the DUT, Agilent 87405C preamplifier is used for increasing sensitivity of the spectrum analyzer. The steps below are followed during the NF measurement:

1) Perform alignment, correlation and calibration for the spectrum analyzer.
2) Place the board on test bench and apply DC bias voltages.
3) Connect RF probes to RF pads and measure the NF with spectrum analyzer. Export required data in csv format and save them into a floppy disc.

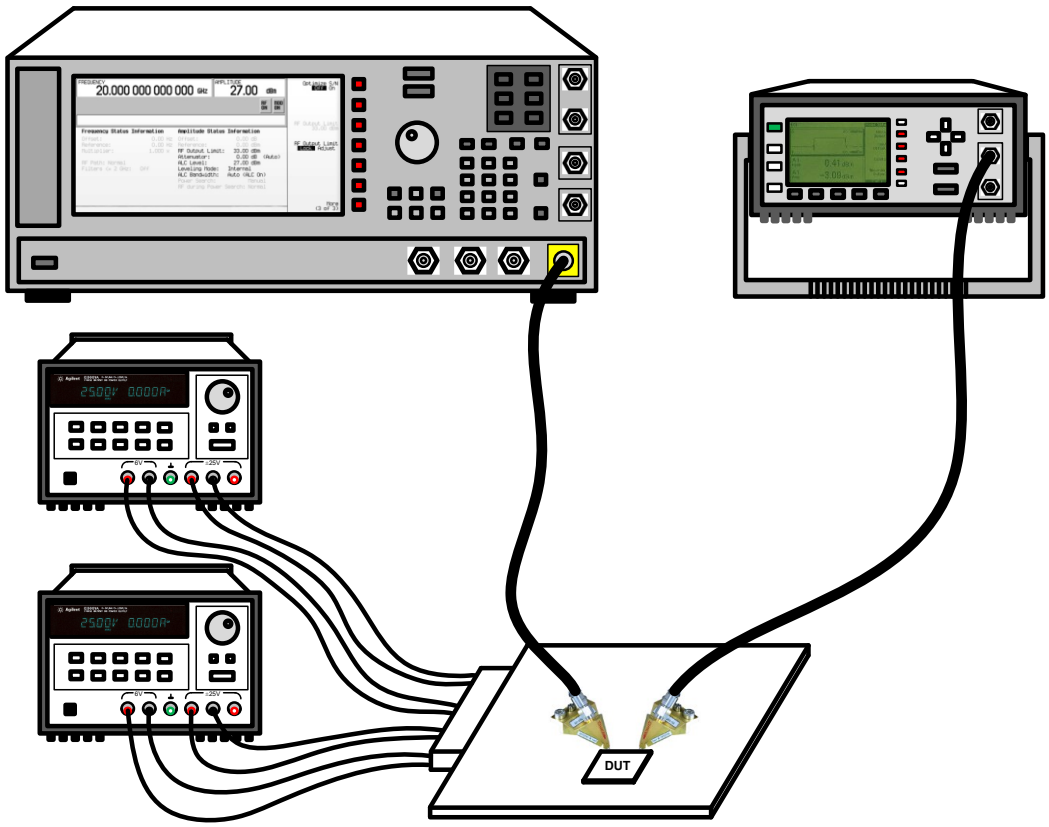

Figure 59: P_{1dB} measurement setup

3. P_{1dB} Measurement

Figure 59 represents simplified diagram of the measurement setup that is utilized for measuring 1-dB compression point of the chips presented in this thesis. Bias voltages are applied via Agilent E3631A DC power supply. RF input is applied by Agilent E3267D 20 GHz PSG Vector Signal generator while the output power is measured by Agilent E4417A power meter. The P_{1dB} measurement procedure is performed by following the steps below:

1) Calibrate the power meter and place the DUT on the test bench while the DC bias voltages are applied.
2) Apply RF input by signal generator and detect the output power with power meter where the difference between applied and measured signal power is equal to S_{21} of the DUT.
3) Sweep the power of RF input and calculate S21 for each of them. The input power at which S_{21} decreases 1 dB from its initial value, is IP_{1dB} of the DUT.