A Wideband High Isolation CMOS T/R Switch for X-Band Phased Array Radar Systems

Emre Özeren *, Arın Can Ulku *, Ilker Kalyoncu *, Can Çalışkan *, Murat Davulcu *, Mehmet Kaynak ^, Yasar Gurbuz *

* Faculty of Engineering and Natural Sciences, Sabanci University, Orhanli, Tuzla, 34956 Istanbul, Turkey, yasar@sabanciuniv.edu

^ IHP microelectronics , Im Technologiepark 25 15236 Frankfurt (Oder), Germany

***Abstract* — This paper presents an SPDT switch which is designed to operate at 8-12 GHz frequency range (X-Band), as a sub module of the front end circuit of a phased array radar. The switch distinguishes itself from its counterparts with its larger frequency range and higher isolation that is uniformly distributed over its bandwidth. It is fabricated using 0.25µm SiGe BiCMOS technology of IHP Microelectronics (Germany). As a new technique, shunt inductors are placed next to shunt transistors in order to improve trade-off between insertion loss and isolation. It has isolation higher than 30 dB in entire band, input referred 1dB compression point is 27.6 dBm, insertion loss is between 2.7-4.1 dB, input and output referred return losses are better than 11 dB in the frequency range of 8-12 GHz.**

***Index Terms* — BiCMOS integrated circuits, SPDT Switch, Transceivers, Phased Arrays**

I. INTRODUCTION

Phased array systems play crucial role in electronic beam control and fast beam scanning for both commercial purposes and defense applications. In order to boost the gain and the effective radiation pattern of the array in desired direction and suppress in other directions, the amplitude and phase of the signals feeding each element are controlled in these systems [1]. Concerning system adaptability and reliability, each antenna element has its own assigned transmit/receive (T/R) module in state of the art X-Band phased array radars [2]. These T/R modules determine the overall performance of RADARs. In a phased array RADAR system thousands of T/R modules are required; therefore, low cost, fully integrated T/R modules are the primary purpose. In these modules, alternation of transmitter mode and receiver mode is realized with a Single pole double throw (SPDT) switch.

A well designed switch conducts the signal to the desired output port with minimal loss, typically less than 4 dB, and isolates the other port from the signal more than 30 dB. Robustness of SPDT switches is also critical in T/R module design, since the switch works continuously regardless of the mode of the radar. In addition, high power handling around 0.5 W is a critical requirement, depending on the particular use of the switch. These performance parameters are the most important figures of merit in a switch, and in operation bandwidth, all of these performance parameters have to meet specifications simultaneously.

Conventionally, T/R modules of phased array radars are designed with III-V technologies for their high performance at radio frequencies. However, recent developments in CMOS and BiCMOS technologies provide a cost effective alternative for fully integrated T/R modules. In this paper we propose a CMOS SPDT T/R switch working in X band (8-12GHz). In design of this SPDT switch, impedance transformation networks (ITN) are utilized, body floating technique and S/D biasing techniques are applied, and as a novelty parallel resonance technique is applied to shunt transistors instead of serial transistors, in order to extend bandwidth in which isolation is higher than 30 dB. The designed switch exhibits a measured IL of 2.7–4.1 dB, isolation from 30 to 35 dB at X-Band with 27.5 dBm IP1dB at 10 GHz, achieving all the performance parameters simultaneously in a wide operation bandwidth.

This paper is organized as follows. Section II presents the design of the T/R switch and techniques to achieve high isolation, low IL and high IP1dB. In Section III layout considerations and measurement results are presented. Finally, section IV summarizes the presented switch.

II. CIRCUIT DESIGN

As shown in Fig.1, the SPDT switch is designed using a series-shunt topology. On/off states of the series NMOS transistors, M1 and M2, determine whether antenna is connected to transmitter or receiver port. The goal of the shunt transistors is to allow the signal that leaked through the off series transistor to be dissipated to the ground, which increases isolation. Isolated NMOS devices are used and bulks of these transistors are biased with 10 kΩ resistances. In order to increase linearity and power handling, ITNs are placed which are formed by L1-C1,

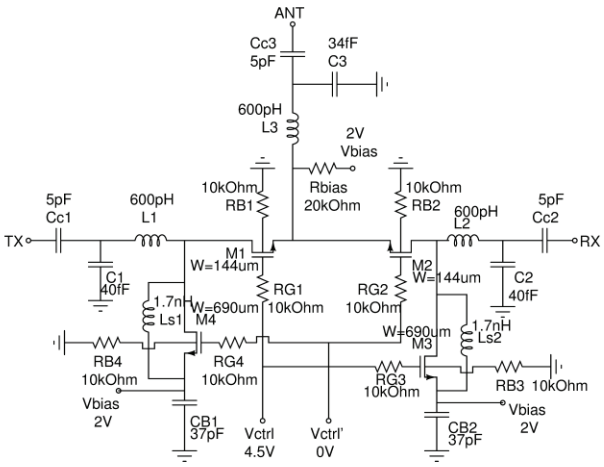

Fig. 1. Circuit schematic of the SPDT switch.

L2-C2 and L3-C3 pairs. Choice of bias voltages are critical to find a middle ground between transistor breakdown voltages and high IP1dB compression point. Taking all these factors into account, the following DC voltage values are chosen as Vbias= 2 V, Vctrl= 6 V, and Vctrl'= 0 V.

Transistor widths are critical to meet both insertion loss and isolation specifications. There is a trade-off between low insertion loss and high isolation. Based on Cadence Virtuoso simulation tools, the optimal widths of the transistors are determined to be 144 µm for M1-M2, and 690 µm for M3-M4.

A noticeable difference between typical series-shunt configuration and this design is the location of the shunt inductor. Normally the shunt inductor is added in parallel to the series transistor, in order to eliminate the capacitive effect of the off transistor by resonating at the central frequency. Presence of the shunt inductor increases the isolation around the central frequency; however it causes poorer performance at frequencies that are further from the center. This topology is not ideal for a wideband switch; therefore the shunt inductor is not added in parallel to the series transistor. Instead, it is located in parallel to the shunt transistor.

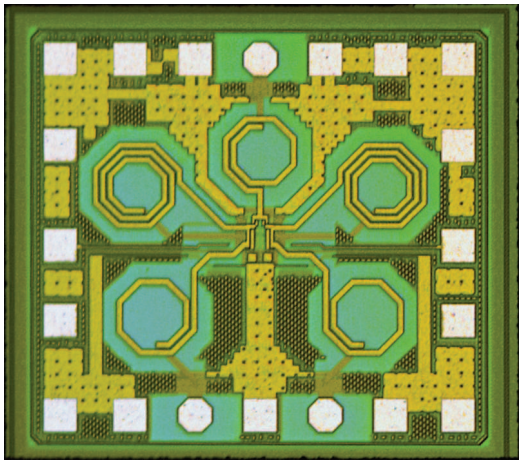

Fig. 2. Die photo of the SPDT switch

When the transistors (M3-M4) are off state, equivalent capacitance from source to drain, Coff, causes leakage. LS1 and LS2 resonate with this Coff to form a high impedance path, reducing this leakage, and improving the trade-off between insertion loss and isolation. To achieve a 10GHz resonance frequency in post layout simulations, 1.7 nH octagonal inductors with the quality factors of ~18 at 10 GHz are used for LS1 and LS2.

III. Measurements

The T/R switch is fabricated in IHP, 0.25-µm SiGe BiCMOS process. The die photo of the switch is shown in Fig. 2. The chip area, including pads, is 0.9 mm2. The thickest top metal layer in the process is used in custom design of inductors due to its lower capacitance to ground and higher conductivity. All inductors are designed with small number of turns and high inner radius for high quality factor with the cost of larger area. These inductors are modeled using Sonnet, and S-parameters of the inductors are extracted to incorporate them to Cadence for post layout simulations. In this topology there are two main elements that increase the area considerably: Presence of shunt inductors, and coupling of two output inductors. In order to avoid coupling of L1 and L2, the distance between is set to more than 290 µm.

S parameter measurement results are presented in Fig. 3. The measured IL and isolation between TX and RX ports is 3.5 dB and 36 dB, respectively, at 10 GHz. IL of the switch is between 2.8 dB and 4.1 dB at X-Band, and isolation is between 30-35 dB at X band. The return loss at TX port, S11, is 16 dB at 10 GHz and changes from 13 dB to 20 dB at X-Band. The return loss at ANT port, S22, is 16 dB at 10 GHz and ranges between 11 dB and 23 dB at X-Band. Due to the symmetry of the switch, IL and RL

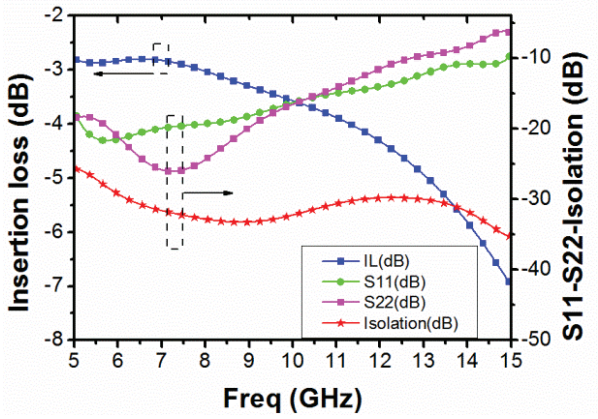

Fig. 3. S parameter measurement results

TABLE I
COMPARISON OF THE SWITCH WITH REPORTED WORKS AT X-BAND.

Ref	Freq. (GHz)	Figures of merit			Chip Area (mm2)	Technique	Tech.
		IL(dB)	Iso. (dB)	IP1dB (dBm)			
This work	8-12	2.8-4.1	30-35	27.5	0.9	**Shunt NMOS-Parallel resonance, body floating, ITN, S/D biasing**	**0.25-µm SiGe BiCMOS**
[6]	8-12	3.2–4.1	23–35	28.2	0.44	Serial NMOS-Parallel resonance, Body floating, ITN, S/D biasing	0.25-µm SiGe BiCMOS
[3]	3–10	3.1±1.3	25–32	18–20	0.62	Distributed topology	0.18-µm CMOS
[4]	3–10.6	2.2–4.2	33–37	-	0.9	Synthetic transmission line	0.25-µm CMOS
[5]	DC-20	0.7	32	25.4	0.06	Synthetic transmission line, body floating and biasing	0.18-µm CMOS
[7]	15	1.8	23	15	0.2	ITNs	0.13-µm CMOS

in the receive mode are almost equal to transmit mode values. As shown in Fig. 4, the switch results in an input 1 dB compression point (IP1dB) of 27.5 dBm at 10 GHz.

Table I compares performance of the presented switch with that of other single-ended CMOS T/R switches reported in the literature, operating at X-Band. High power handling (> 0.5 mW), low insertion loss (<4 dB), high isolation (>30 dB) are needed to be achieved simultaneously in operation bandwidth. Only in this presented switch and [6] meets these specifications at X-Band. In comparison with [6], which is a very similar work, this SPDT has lower IL and higher isolation. This work provides higher isolation in a wider bandwidth, and it is achieved by changing the location of the parallel resonance from series transistor to shunt transistor.

IV. CONCLUSION

This paper presented a high linearity and high isolation X-Band T/R switch which is fabricated in 0.25µm SiGe BiCMOS technology. It exhibits an IL of 3.5 dB, isolation of 36 dB and P1dB of 27.5dBm at 10GHz. The single-ended CMOS T/R switch presented in this paper shows the competitive P1dB and isolation, and comparable IL with state of the art at X-Band. Improvement in trade-off between insertion loss and isolation in a wide bandwidth is achieved by changing the location of the parallel resonance from series transistor to shunt transistor.

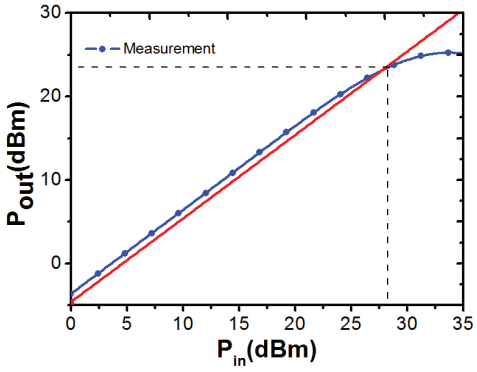

Fig. 4. Measured 1-dB compression point (IP1dB) of the switch at 10 GHz.

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