A PFM based Digital Pixel with Off-Pixel Residue Measurement for 15µm Pitch MWIR FPAs

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ABSTRACT

Digital pixels based on pulse frequency modulation (PFM) employ counting techniques to achieve very high charge handling capability compared to their analog counterparts. Moreover, extended counting methods making use of left-over charge (residue) on the integration capacitor help improve the noise performance of these pixels. However, medium wave infrared (MWIR) focal plane arrays (FPAs) having smaller pixel pitch are constrained in terms of pixel area which makes it difficult to add extended counting circuitry to the pixel. Thus, this paper investigates the performance of digital pixels employing off-pixel residue measurement. A circuit prototype of such a pixel has been designed for 15µm pixel pitch and fabricated in 90nm CMOS. The prototype is composed of a pixel front-end based on a PFM loop. The front-end is a modified version of conventional design providing a means for buffering the signal that needs to be converted to a digital value by an off-pixel ADC. The pixel has an integration phase and a residue measurement phase. Measured integration performance of the pixel has been reported in this paper for various detector currents and integration times.

Keywords: analog to digital converter, extended integration, off-pixel residue, pulse frequency modulation, medium wave infrared, focal plane array

1. INTRODUCTION

Successful implementations of pixel sensors for infrared focal plane arrays (IR-FPAs) have been demonstrated many times in the literature. Both analog and digital versions of such pixel sensors can be found [1-5]. The analog sensors offer a larger fill factor, whereas digital pixel sensors (DPS) provide a direct digital output and can significantly improve the charge handling capability [2]. Generally, a DPS either consists of an in-pixel analog-to-digital converter to perform the signal conversion or it is based on a pulse frequency modulation (PFM) loop. While the former applies direct analog-to digital conversion to the pixel, the latter incorporates multiple-self-reset operation using a comparator. PFM-based designs have shown better signal-to-noise ratio (SNR) and dynamic range performance[6]. Recently, a number of applications for FPAs requiring small pixel pitches in the medium-wave infrared (MWIR) regime have emerged [7]. Smaller pixel pitch means that the pixel real estate is constrained in terms of area. In this case, analog pixels are usually preferred due to their superior fill factor. Analog pixels however, have shown poor SNR performance. Traditional DPSs on the other hand can provide significant improvement in the SNR at the cost of increased pixel area, though not at low illumination levels. A need therefore arises to develop pixel architectures that can alleviate SNR performance at low illumination while occupying smaller area.

Traditional PFM based implementations of DPSs store charge in the digital domain resulting in the charge handling capacity increasing exponentially with respect to pixel area contrary to the linear scaling in case of conventional analog pixels. These pixels typically consist of a front-end based on a PFM loop, counters and memory.

Such PFM implementations are reported[8-10] where excellent imaging results are obtained but only for higher illumination levels when the detector current is large. An extended counting technique has been proposed[2] where the left-over charge on the integration capacitor is computed (converted to digital) in-pixel and then stored in in-pixel memory as well. This computation is carried out by counting the number of clocks from the time when integration is stopped till the next auto-

Infrared Technology and Applications XLII, edited by Bjørn F. Andresen,
Gabor F. Fulop, Charles M. Hanson, Paul R. Norton, Proc. of SPIE Vol. 9819,
981929 · © 2016 SPIE · CCC code: 0277-786X/16/$18 · doi: 10.1117/12.2224791

reset. The additional bits obtained from this computation are added to the pixel count. The drawback of this technique is the larger pixel area. The single pixel design[2] was for a 30µm pixel pitch. With smaller pixel sizes such as 15µm pitch the required additional circuitry for extended counting cannot fit within the pixel area.

In this brief, the idea of residue measurement to improve SNR has been exploited and a digital pixel which is a modified version of the conventional PFM architecture has been proposed along with a method to measure residue outside the pixel. A prototype has been developed as a proof of concept. The aim is to achieve the superior SNR performance of digital pixels for smaller pixel pitch by delegating the residue measurement job to an off-pixel ADC. SNR has been measured and reported.

The paper is organized as follows: Section 2 describes a conventional PFM based pixel and provides background on the extended counting technique[2], Section 3 describes the architecture of the proposed pixel. Measurement results are shown in Section 4 and finally the concluding remarks are provided in Section 5.

2. DIGITAL PIXEL IMPLEMENTATIONS

2.1 Conventional PFM based Pixel

Schematic of the pixel front-end is shown in Figure 1. This is a conventional pixel architecture based on a PFM loop. Detector current (or photocurrent) is emulated by the current supplied by current source device M1 along with direct injection (DI) device M2. This current fills up the capacitor C at a speed determined by incoming current. Once the voltage at node A exceeds Vref, the comparator switches to high and M3 turns on. This resets the capacitor to 0V and the integration operation continues. The 4 inverters in the loop create delay to ensure that the capacitor gets enough time to discharge completely.

Every time the comparator switches, a short pulse is generated at node P, this is termed as the PFM signal. This signal is fed to a counter as its clock. The integration operation continues till a manual reset signal turns M4 on. When this happens, the capacitor is discharged to 0V and at this point the counter holds the digital value corresponding to the integration time and eventually the number of charges collected. This count value is transferred to a memory in the form of a register. Period of this reset signal defines the duration of integration phase.

Figure 2 illustrates the operation of the pixel front-end. As shown in figure, the residue, which corresponds to the remaining charge on the capacitor at the end of the integration period, is essentially wasted. The extended integration method proposed[2] makes use of this left-over charge to improve the overall SNR of such a DPS for scenarios where detector illumination is low and hence the current is low. Next section provides quick snapshot of the extended counting technique.

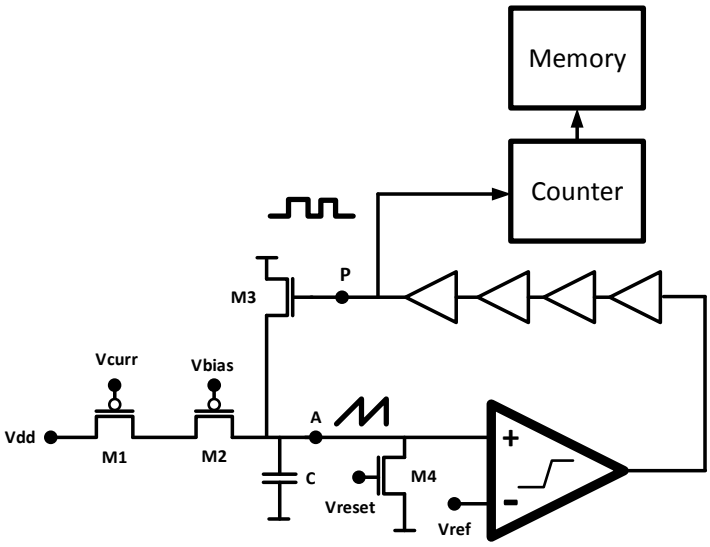

Figure 1. Schematic of a conventional PFM-based digital pixel

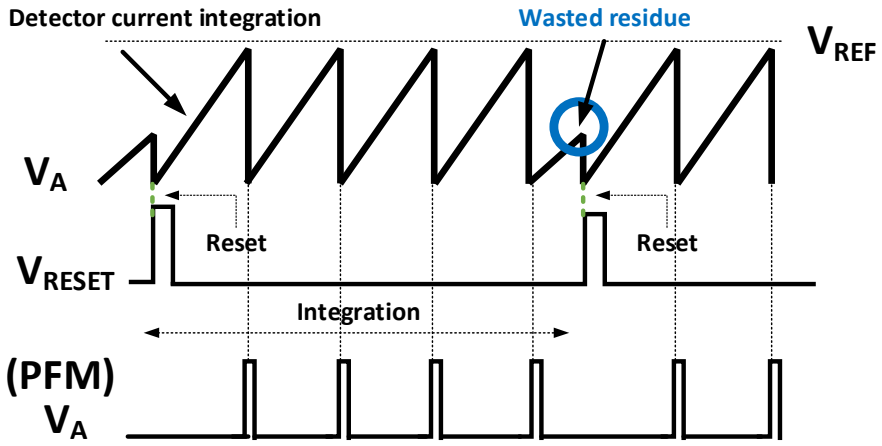

Figure 2. Timing and operation of a conventional digital pixel

2.2 Pixel based on Extended Counting

In extended counting[2], the integration phase is the same as in a conventional PFM-based DPS explained in previous section. However, with added residue phase to the pixel's operation where value of the left-over charge on the integration capacitor is calculated by the use of the same counter but with a different clock which is much faster than the PFM signal [2]. This phase is termed as the fine quantization phase which makes integration the coarse quantization phase. This phenomenon is same as seen in a sub-ranging ADC where the signal range is reduced after a coarse quantization step and then further conversion is performed on the remaining signal. Therefore, during fine quantization, conversion of this left-over charge (or voltage) is measured by synchronous mode of operation of the same counter to trigger the comparator one more time. The residue enable signal shown in Figure 3 is responsible for switching between integration and residue phases.

Integration of the photocurrent onto the integration capacitor is allowed to continue during the residue phase even though integration has logically ended. This counting is done till the next auto-reset event occurs at which point the residue data is transferred to a register. An arithmetic logic unit (ALU) then performs the computation combining primary count and the residue value obtained to generate the final output[2].

This technique produces excellent results, especially at low illumination levels where the improvement in SNR is significant. However, the additional logic required to perform residue computation and the extra storage registers increase the pixel area. As mentioned earlier, for FPAs having smaller pixel pitches of 15µm it would be hard to accommodate this much real estate to the pixel electronics.

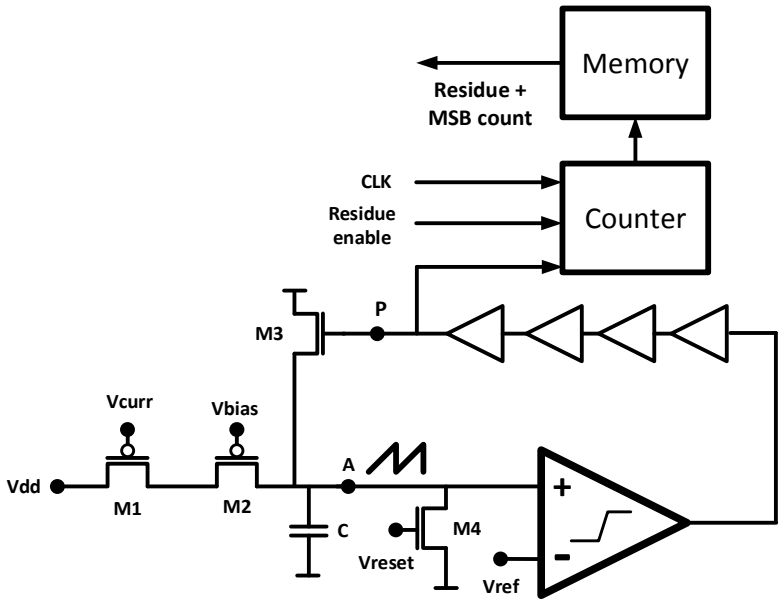

Figure 3. Pixel architecture for implementing PFM with extended integration[2].

3. PROPOSED ARCHITECTURE

For the area constraints of a 15µm x15µm size pixel, using the extended counting technique for measuring residue does not seem feasible for this work. To this end, a method is proposed where a modified PFM-based pixel architecture is used for the front-end whereas residue measurement is performed off-pixel using a column ADC. Primary count giving MSB is carried out the same way as in a conventional architectural. For MWIR spectrum, a 5-bit MSB counter meets the required charge handling specification with the given area constraints.

The ADC performs a direct conversion on the residue voltage and the digital value obtained is simply appended to the MSB count value. From computational point of view, this method has a certain degree of simplicity compared to the extended counting[2] method because no additional computations are required for residue bits and thus eliminating the need of an ALU. However, accuracy of the measured residue for this method is limited by the performance of the ADC. Moreover, the power consumption of each ADC adds to the total power budget.

Major modifications to the pixel include the addition of a source follower and the use of a power efficient self-biased differential amplifier instead of the comparator. In Figure 4 part of the full pixel front-end has been shown with the proposed modifications highlighted.

As shown in Figure 5, the instant at which integration is stopped, the amount of residue charge (or voltage) is sampled by the ADC. In a design with a full 2D array, this residue charge is required to be held on the integration capacitor before reset is applied. This will require minor changes in the design of the pixel front-end.

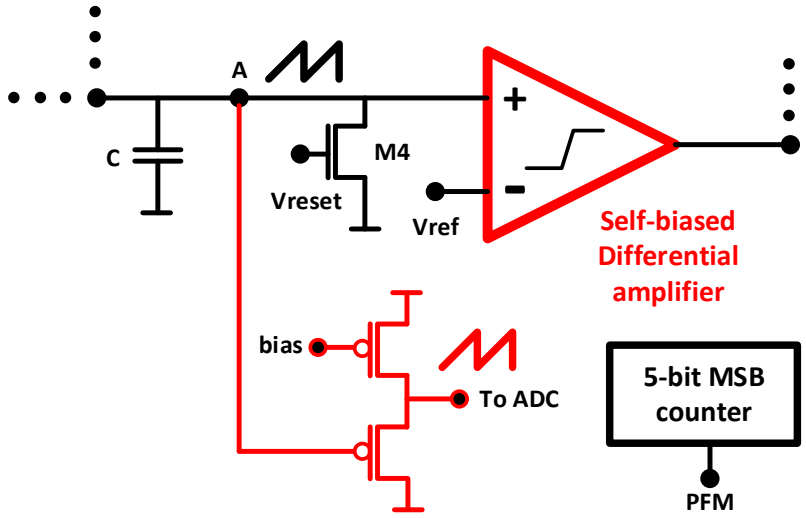

Figure 4. Proposed modification to a conventional PFM-based digital pixel

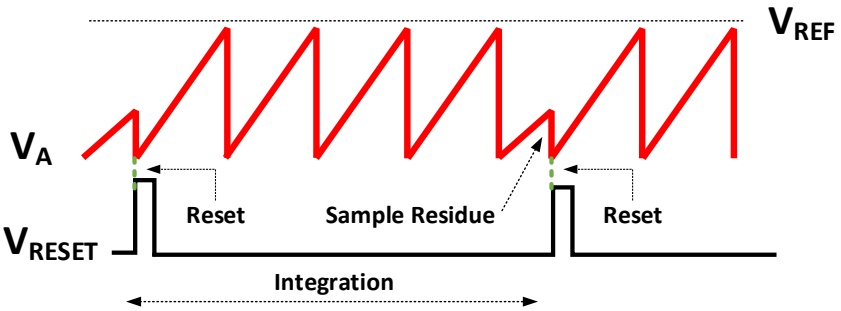

Figure 5. Timing operation of proposed pixel with integration and residue phase

3.1 Buffer

Delegating the residue measurement job to an off-pixel circuit requires proper buffering at node A because this node is very sensitive and can be easily loaded by the ADC. This is done by adding a source follower inside the pixel as shown in Figure 4. Source follower is a very simple and concise circuit that can provide decent buffering performance and without consuming much area. Adding the source follower does result in a level-shift of the integration (saw tooth) waveform though, but this can be handled by adjusting reference voltage of ADC.

3.2 Comparator

Comparator design have no a direct impact on the performance of a given residue measurement method but provided that off-pixel ADCs will add to the overall power consumption, a power efficient front-end pixel design is needed. Furthermore, it is well known that power consumption of a PFM-based pixel is dominated by the dynamic elements in the PFM loop which include the inverters and comparator[2]. Therefore, besides the addition of a source follower in the modified pixel, a new comparator in the form of a power efficient self-biased differential amplifier has been added. The amplifier works as a pseudo comparator. It amplifies the difference between the voltage on the integration node and reference voltage Vref. This difference voltage then drives the feedback inverters to generate the PFM signal. Figure 6 shows the schematic of the designed amplifier. The self-biased topology also helps to eliminates additional bias voltage from the front-end pixel circuit.

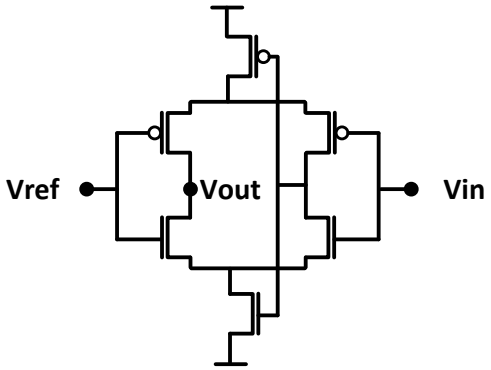

Figure 6. Self-biased power efficient differential amplifier as Pseudo Comparator

4. MEASUREMENTS AND RESULTS

Output of the pixel front-end (i.e. output of the source follower buffer) has been measured by controlling the manual reset input with a logic analyzer. These measurements have been done for various currents and integration durations. Fig. 7 and Fig. 8 show the measurement results with a 170 µs integration time with 300 pA current and 170 µs integration time with 600 pA current respectively.

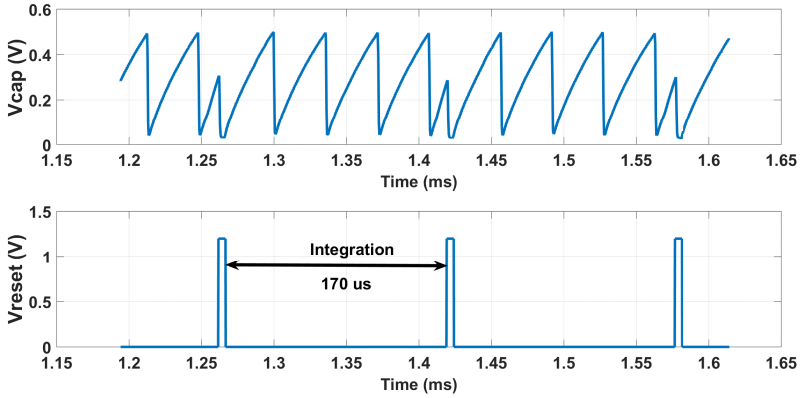

Figure 7. Measured pixel operation with an input current of 300 pA. Vcap corresponds to node A in Figure 4

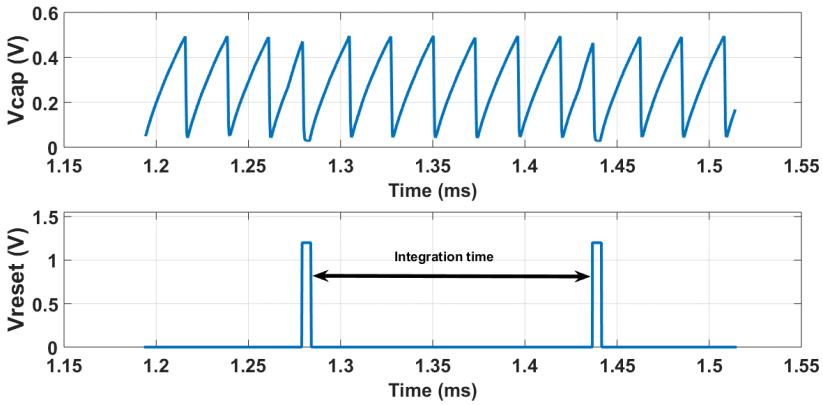

Figure 8. Measured pixel operation with an input current of 600 pA. Vcap corresponds to node A in Figure 4

5. CONCLUSION

A first prototype of a DPS, intended for small pixel pitch for MWIR FPAs, with off-pixel residue measurement has been reported. A test setup comprising of a designed and fabricated modified PFM based pixel with an off-pixel (and off-chip) ADC, counter and comparator provides a sense of feasibility of the proposed method. The SNR results of single pixel are encouraging and will provide a strong platform for the next prototype which is the design of FPA with column ADCs performing the residue measurement/conversion.

ACKNOWLEDGEMENT

The authors would like to thank TUBITAK, The Scientific and Technological Research Council of Turkey, for funding this project. The work was carried out under project grant 113E598.

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