

A High Performance Hardware for Early Terminated C-1BT Based Motion Estimation

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Abstract—Motion Estimation (ME) is the most computationally intensive part of video compression systems. In this paper, a high performance hardware for early terminated constrained one-bit transform (C-1BT) based low bit depth ME is proposed. The proposed early terminated C-1BT based ME hardware can process more than 30 quad full HD (3840x2160) video frames per second. The early termination algorithm reduced the energy consumption of the proposed ME hardware by 26%.

Keywords—*Motion Estimation, One Bit Transform, Early Termination, Hardware Implementation, FPGA.*

I. INTRODUCTION

Motion Estimation (ME) is the most computationally intensive part of video compression systems [1]. Therefore, several low bit depth representation based ME methods are proposed to reduce the computational complexity of ME. In [2], one-bit transform (1BT) based ME is proposed. It converts full bit depth video frames into one-bit depth frames by comparing original frames with multi-band pass filtered versions of the original frames. Therefore, it uses Exclusive-OR (EX-OR) based matching criterion instead of the conventional Sum of Absolute Difference (SAD) matching criterion. In [3], a new multi-band pass filter kernel is proposed for 1BT to facilitate a multiplication free transform for reduced transform complexity. This is called multiplication-free one-bit transform (MF1BT) based ME. Constraint one-bit transform (C-1BT) based ME proposed in [4] tries to determine the reliable pixels in one-bit frames by using another bit plane called constraint mask (CM).

There are several hardware implementations of low bit depth ME methods in the literature [2, 5, 6, 7]. The first 1BT based ME hardware implementation in the literature is presented in [2]. In [2], a motion vector (MV) based linear arrays hardware architecture is used for implementing 1BT based ME. In [5], a source pixel based linear arrays hardware architecture is used for implementing MF1BT based ME. In [6], a 1BT based ME hardware searching 4 macro blocks (MB) in parallel with a novel data re-use scheme is proposed to increase performance and reduce on-chip memory usage. In [7], a high performance reconfigurable hardware for 1BT based multiple reference frame (MRF) ME is proposed.

In this paper, a high performance hardware for early terminated C-1BT based low bit depth ME is proposed. The

proposed early terminated C-1BT based ME hardware can process more than 30 quad full HD (3840x2160) video frames per second. The early termination (ET) algorithm reduced the energy consumption of the proposed ME hardware by 26%.

In the proposed ME hardware, ET algorithm proposed in [8] is used. This algorithm checks the activity of the current block. If block activity is low, MVs of neighboring blocks are used to determine MV of the current block. If block activity is high, full search ME is performed for the current block. If the original frame has smooth content, the corresponding pixels in CM are 0. Therefore, if the sum of CM values of pixels in a block is less than a threshold, then ET is decided. This can be formulated as shown in (1). In this equation, α is a normalization parameter. If the condition in (1) is satisfied, the median of MVs of the left, upper, and upper-left blocks is assigned as MV of the current block. Otherwise, full search ME is performed for this block. This ET algorithm reduces the computational complexity of C-1BT based ME by on average 25% with a very small PSNR loss. Since it uses a part of the already available matching criterion and simple arithmetic operations to determine the activity of the current block, it has significantly less computational complexity than the previous ET algorithms proposed for low bit depth ME.

$$\sum_{i=0}^N \sum_{j=0}^N CM^t(i, j) < \frac{N \times N}{\alpha} \quad (1)$$

II. C-1BT BASED ME HARDWARE

The proposed C-1BT based ME hardware is based on the fixed block size (FBS) single reference frame (SRF) ME hardware proposed in [7]. The C-1BT based ME hardware is more complex and has higher on-chip memory requirement than the 1BT based FBS SRF ME hardware. Same as the FBS SRF ME hardware, C-1BT ME hardware finds MVs of four 16x16 MBs in parallel using full search ME algorithm. Therefore, their throughputs are the same. However, the C-1BT based ME hardware uses the minimum CNNMP criterion instead of the NNMP criterion.

The datapath of the proposed C-1BT based ME hardware is very similar to the FBS SRF ME hardware proposed in [7]. It searches for four MBs (MB0, MB1, MB2 and MB3) in parallel. The FBS SRF ME hardware proposed in [7] searches for the current MB only in a 1-bit depth search window (SW).

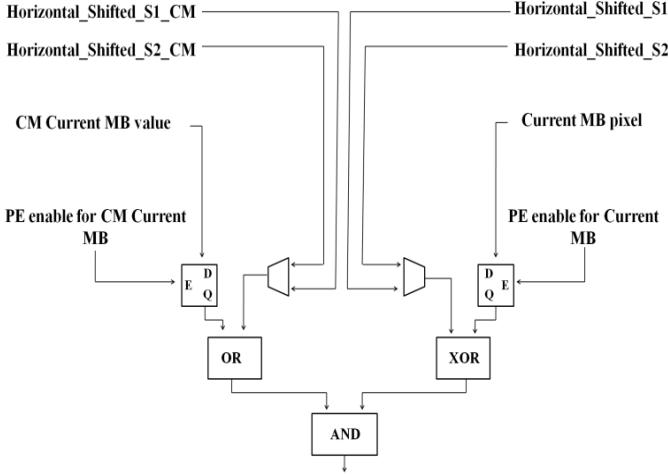


Fig. 1. PE Architecture

But, the C-1BT based ME hardware also requires searching in CM SW. Therefore, the number of BRAMs and horizontal shifters are increased from 2 to 4. In the proposed C-1BT based ME hardware, the same search locations in the CM and 1-bit depth image are searched in parallel. Therefore, the control signals used for BRAMs and Horizontal Shifters are the same as the control signals in [7].

Same as the FBS SRF ME hardware proposed in [7], C-1BT based ME hardware uses four 256 processing element (PE) arrays. But, PE architectures are different. In the C-1BT based ME hardware, both the CM values and 1-bit depth pixels are used during the search process. Therefore, CM values are sent to the PE arrays together with the 1-bit depth pixels. This is the main difference between the PE arrays in [7] and the PE arrays in C-1BT based ME hardware.

The architecture of a PE used in C-1BT based ME hardware is shown in Fig. 1. Each PE performs XOR operation between a SW pixel from the 1-bit depth reference image and a current MB pixel from the 1-bit depth current image, OR operation between a corresponding SW value from the reference CM and a corresponding current MB value from the current CM, and then AND operation between the results of the XOR and OR operations. The result of the AND operation indicates whether the SW pixel and the current MB pixel match or not. CNNMP values for each row of the MB are computed by using Non-Match Counters (NMCs) as in [7]. These count the ones in the outputs of the 16 AND gates by using 4 look up tables with 24 entries and sum the outputs of these look up tables. The results of these 16 NMCs are accumulated to compute the CNNMP value for a search location. Therefore, 64 NMCs are used in the proposed C-1BT based ME hardware for computing CNNMP values of four MBs in parallel.

Before ME starts for a MB, SW pixels of 4 neighboring MBs (SWT) from the 1-bit depth reference image are loaded to two dual-port BRAMs (BRAM0 and BRAM1) in the FPGA, and the corresponding SWT values from the reference CM are loaded to two dual-port BRAMs (BRAM2 and

BRAM3) in the FPGA. The memory organization of the 64x64 SWT pixels from the 1-bit depth reference image is as in [7]. The memory organization of the 64x64 SWT values from the CM is similar to this memory organization. The left 32 bits of the CM values are stored in BRAM2 and right 32 bits are stored in BRAM3.

III. EARLY TERMINATED C-1BT BASED ME HARDWARE

The proposed C-1BT based ME hardware is modified for implementing the early terminated C-1BT based ME algorithm. As shown in Fig. 2, ET decision hardware is added to the C-1BT based ME hardware. The ET decision hardware starts working during data loading, before the search process starts. While the current MB CM values of the four MBs are loaded from the off-chip memory to the PE arrays, ET decision hardware also takes these values and starts determining MBs to be early terminated. It decides the early terminated MBs before loading SWT pixels from off-chip memory to BRAMs finishes. After it decides the early terminated MBs, it sends this information to the comparator & MV generator, control unit and PE array. It avoids switching activities for the early terminated MBs until data loading for the next four MBs starts.

The proposed early terminated C-1BT based ME hardware searches four MBs in parallel. Therefore, it increases the performance of the C-1BT based ME hardware when these four MBs are early terminated. If ET decision hardware determines that these four MBs will be early terminated, the comparator & MV generator hardware calculates the MVs of the early terminated MBs, and then the search process starts for the next four MBs. If at least one of these four MBs is not early terminated, the performance of the C-1BT based ME hardware does not increase. However, in this case, the control unit stops the switching activities in the PE Arrays of the early terminated MBs in order to reduce power consumption.

Switching activities in PEs, adder trees and comparators are reduced for early terminated MBs during the search process. PE Array used in early terminated C-1BT based ME hardware has additional multiplexers compared to PE Array used in C-1BT based ME hardware. When a MB is early terminated, 0 is sent to PE Array for both the SWT of 1-bit depth image and CM.

ET decision hardware architecture is shown in Fig. 3. The ET decision hardware starts working while CM values for the current MB are loaded from the off-chip memory to the PE arrays. The number of “1”s in a row of CM for the current MB is calculated using NMC hardware. The NMC hardware architecture is as in [7]. Accumulators shown in Fig. 3 calculate the total number of “1”s in CM for the current MB in 16 clock cycles. The ET decision hardware also calculates the total number of “1”s in CM of the current image. This value is used for calculating α for the next image. Calculating α requires division and multiplication operations. In the proposed hardware, these division and multiplication operations are implemented using addition and shift operations. After α is calculated, $(N \times N) / \alpha$ is calculated. This

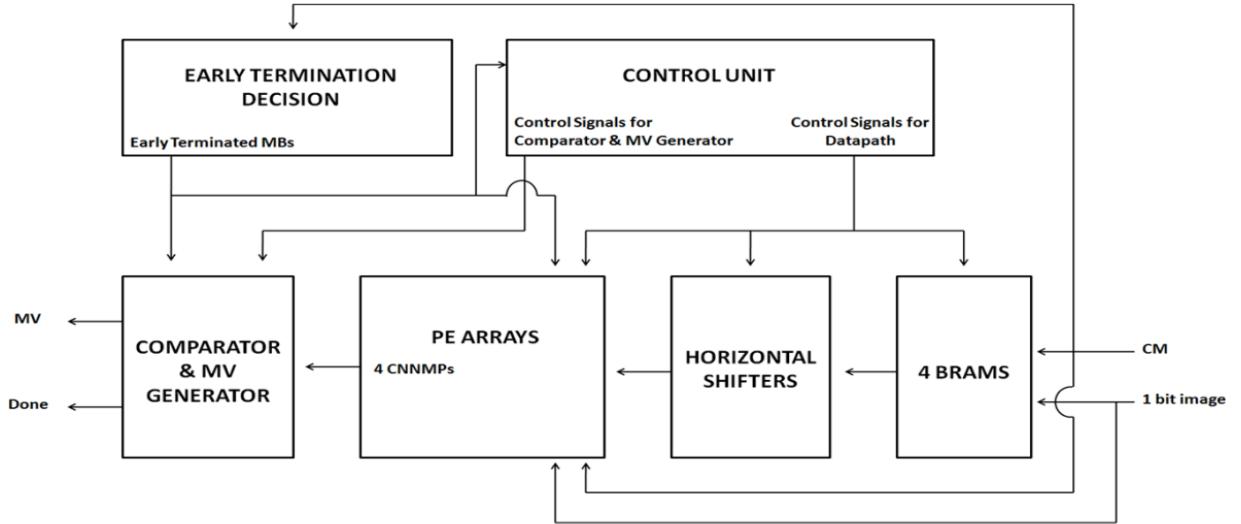


Fig. 2. Top-Level Block Diagram of the Proposed Early Terminated C-1BT ME Hardware

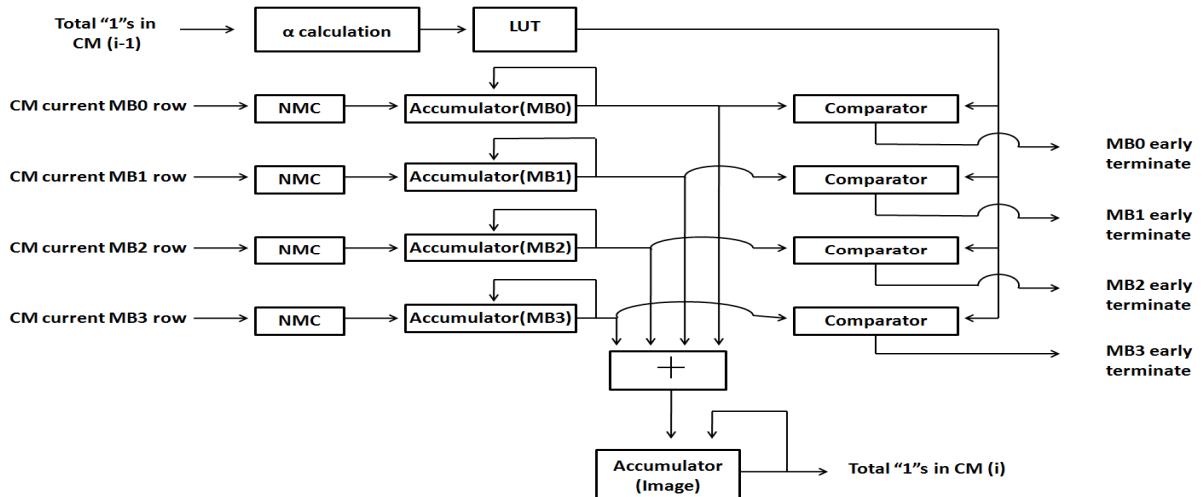


Fig. 3. Early Termination Decision Hardware

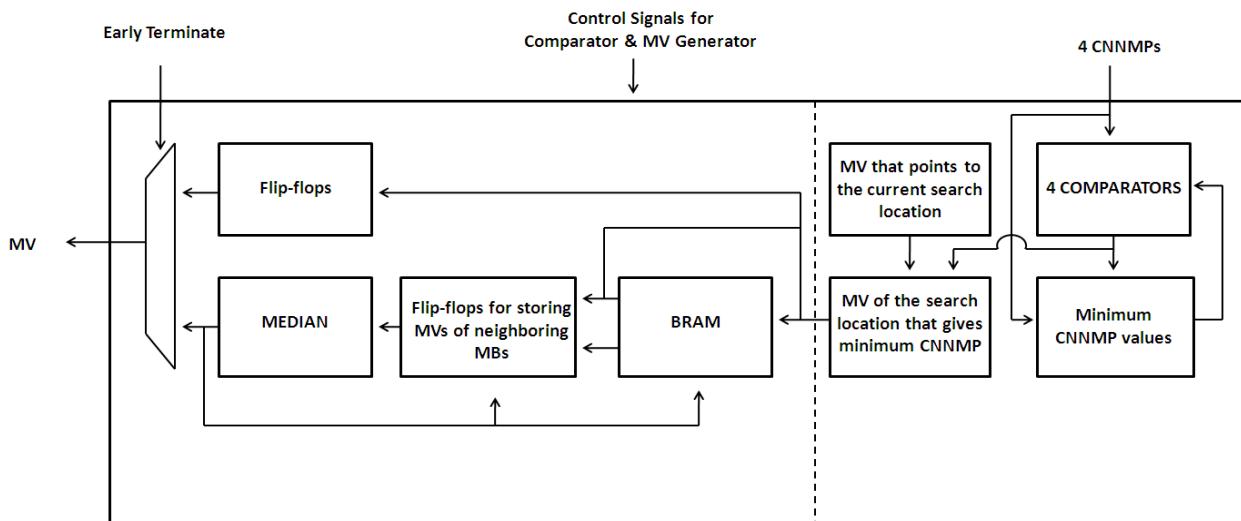


Fig. 4. Comparator & MV Generator Hardware for Early Terminated C-1BT ME Hardware

TABLE I. HARDWARE COMPARISON

	C-1BT ME Hardware	Early Terminated C-1BT ME Hardware
Bit Depth	2	2
On-Chip Memory (bits)	8192	9632
Area	4529 LUTs 3667 DFFs	5035 LUTs 4100 DFFs
Maximum Frequency (MHz)	270	265
Search Range	[-16, 16]	[-16, 16]
Search Location / MB	1089	1089
Percentage of Early Terminated MBs	—	50.54%
Percentage of 4 MBs Processed in Parallel Early Terminated	—	86.32%
Dynamic Power Consumption (mW)	160	202
Time (ms)	26.21	15.22
Energy Consumption (mJ)	4.193	3.074
Energy Reduction	—	26.69%

calculation is implemented using look up tables (LUT). N is set to 16 in the proposed hardware implementation. The outputs of the LUTs are compared with the final values in the accumulators. If total number of “1”s in CM of a MB is less than the output of the LUT, the ET decision hardware decides that the search process will be skipped for this MB.

The comparator & MV generator hardware architecture is shown in Fig. 4. The left part of the dashed line is the hardware used for computing the MVs of the early terminated MBs. In the C-1BT based ME hardware, the MV pointing to the search location with the minimum CNNMP is taken as the MV of the corresponding MB. However, in early terminated C-1BT based ME hardware, MVs of the left, upper, and upper-left neighboring MBs are used to calculate the MVs of early terminated MBs. Therefore, the MVs of these neighboring MBs are stored in BRAMs. If a MB is early terminated, the multiplexer at the output of the comparator & MV generator selects the output of median hardware as the MV of this MB.

IV. IMPLEMENTATION RESULTS

The proposed C-1BT based ME and early terminated C-1BT based ME hardware architectures are implemented in Verilog HDL. The Verilog RTL codes are mapped to Xilinx XC5VLX110T FPGA. The FPGA implementations are verified with post place and route timing simulations. The implementation results are shown in Table I.

The C-1BT based ME hardware uses 4096 bits on-chip memory for storing SWT pixels from the 1bit depth image and 4096 bits on-chip memory for storing SWT values from CM. Therefore, it requires 8192 bits on-chip memory. These 8192 bits are stored in 64 addresses of 4 BRAMs. Same as the FBS SRF ME hardware proposed in [7], 1127 clock cycles are required by the proposed C-1BT based ME hardware for processing four MBs in a [-16, 16] search range. The proposed C-1BT based ME hardware implementation can work at 270

MHz. Therefore, it is capable of processing 30 quad full HD (3840x2160) video frames per second.

The early terminated C-1BT based ME hardware requires more LUTs and DFFs than the C-1BT based ME hardware. It stores MVs of the MBs of a row of the image in order to calculate the MVs of the early terminated MBs. Therefore, it uses 1440 bits additional on-chip memory. 1 BRAM is used for storing these 1440 bits. Therefore, it requires 9632 bits on-chip memory. The ET decision hardware works in parallel with the C-1BT based ME hardware. The calculation of the MVs for early terminated MBs requires additional 4 clock cycles. However, the calculation of the MVs for early terminated MBs is done in parallel with the first 4 clock cycles of ME process for the next four MBs. Since the ET decision and comparator & MV generator hardware work in parallel with C-1BT based ME hardware, in the worst case, early terminated C-1BT based ME hardware is capable of processing 30 quad full HD video frames per second. The proposed early terminated C-1BT based ME hardware searches four MBs in parallel. When these four MBs are early terminated, it can process more than 30 quad full HD video frames per second.

The dynamic power consumptions of both hardware implementations on the same FPGA are estimated using Xilinx XPower tool. Timing simulation of the placed and routed netlist of each hardware implementation is done for one frame of Park Joy full HD video at 100 MHz and the signal activities are stored in a Value Change Dump (VCD) file. This VCD file is used for estimating the power consumption of that hardware implementation. The results show that early terminated C-1BT based ME hardware consumes more dynamic power than C-1BT based ME hardware, because ET decision hardware and comparator & MV generator hardware work in parallel with C-1BT based ME hardware. However, early terminated C-1BT based ME hardware is faster than the C-1BT based ME hardware. Therefore, it has 26% less energy consumption than the C-1BT based ME hardware.

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