A Fully Integrated Low-Power SiGe Power Amplifier for Biomedical Applications

Journal:	*IET Microwaves, Antennas & Propagation*
Manuscript ID:	MAP-2009-0437.R3
Manuscript Type:	Research Paper
Date Submitted by the Author:	n/a
Complete List of Authors:	Kaynak, Mehmet; Sabanci University, FENS Gurbuz, Y; Sabanci University, Electronics Engineering
Keyword:	BIOMEDICAL ELECTRONICS, POWER AMPLIFIERS, ANALOGUE INTEGRATED CIRCUITS, TRANSMITTERS

A Fully Integrated Low-Power SiGe Power Amplifier for Biomedical Applications

Mehmet Kaynak, Ibrahim Tekin and Yasar Gurbuz
Sabanci University, Faculty of Engineering and Natural Sciences, Tuzla, 34956, Istanbul, Turkey
Tel: +90(216) 483 9533, e-mail: yasar@sabanciuniv.edu

Abstract— **In this work, a full-integrated very-low power SiGe Power Amplifier (PA) is realized using the IHP (Innovations for High Performance), 0.25µm-SiGe process. The behaviour of the amplifiers has been optimized for the 2.1-2.4 GHz frequency band for a higher 1-dB compression point and high efficiency at a lower supply voltage. The PA delivers an output power of 3.75 mW and 1.25 mW for 2V and 1V, respectively. The PA measurements yielded the following parameters; gain of 13 dB, 1-dB compression point of 5.7 dBm, and Power-Added-Efficiency of 30% for 2V supply voltage. The PA circuit can go down to 1V of supply voltage with a gain of 10 dB, 1-dB compression point of 1 dBm, and Power-Added-Efficiency of 20%. For both supply voltages, the input and the output of the circuit give good reflection performance. With this performance, the PA circuit may be used for low-power biomedical implanted transceiver systems.**

***Keywords*—** Power Amplifier, low-power IC, Biomedical**,** SiGe

I. INTRODUCTION

Recent developments in radio frequency integrated circuit (RFIC) technologies have resulted in their increasing application in implantable wireless biomedical systems. Use of the human body as a wireless communication channel is the major challenge to the realization of an implanted RF transceiver system. It has been shown that the biological tissues are not a good medium at RF frequencies due to their dissipative characteristics. One way to overcome this problem is to realize a particularly efficient wireless transmitter. One of the major challenges to realize these transmitters is to design RF circuits, and in particular power amplifiers (PAs) with low-power consumption that operate from very low supply voltages. However, having a low supply voltage degrades the linearity performance of the amplifier. Class A, Class B or Class AB PAs are good candidates to provide solutions to the linearity problem [1]. The challenging part of these amplifiers is the efficiency, which directly affects the battery life. Using cautious design methods, such as optimization of the passive components and decreasing the passive element losses, helps designers to achieve high PAE Class A or AB amplifiers. DC-feed inductors are the most important

components which directly affect the efficiency of the amplifier. Since low-power PAs require larger output loads than higher-power PAs, larger DC-feed RF inductors are required; but such inductors have very low quality factors when implemented on-chip. A special design is required for the DC-feed inductor to simultaneously obtain higher efficiency and linear operation. Using all the active components parasitic elements and using all the metallization as a part of the matching network also helps to increase efficiency by decreasing unnecessary losses. All these topics are related to the layout design.

A few fully integrated PAs with high output power levels in the range of 1 to 2 Watts and with efficiencies ranging from 13-44 % have been presented [2-5]. On the other hand, good performance for low-power and linearity, and fully integrated PAs that operate from low supply voltages have not been reported yet. The switching-class PAs require a large input drive and are highly nonlinear. Thus, their suitability for low-power applications is still being debated [6-8]. This work investigates the use of linear-class PAs for low-power, short-range biomedical applications. A PA circuit operating at 2.4 GHz was designed and fabricated in a commercial 0.25 μm SiGe process [9]. Although the circuit has a basic topology of a single class-A stage, the optimized layout of the circuit allowed us to achieve a measured performance, superior to those of other reported fully integrated low-power PAs. This PA circuit is capable of operating at a supply voltage as low as 1 V with 20 % PAE, proving that linear class PAs are good candidates for biomedical implants.

II. Design of Power amplifier and Matching Circuits

Error! Reference source not found. shows the schematic view of the single-stage power amplifier. Despite the fact that differential amplifiers have better CMRR performance, the single-ended PA topology was chosen to be used with a single-ended antenna, thus eliminating the need for a balun. In the case of low-power signals, no driver stage is required for the design of the power amplifier. An input matching network is used to match the input of the PA to 50 Ω. The inductance value required for the matching network is larger since the input transistor Q_1 is a smaller device, and therefore has a low input capacitance which has a negligible effect at the frequency of interest. The emitter inductance (L_e) is used for increasing the real part of the input impedance thus making the input matching easier and also increasing the linearity of the amplifier. The base of Q_1 was biased in the class-A operation range to ensure the

linear operation. A custom, thermal-sensitive bias circuit is applied for DC biasing of the amplifier. The capacitor C_1 is a DC-blocking capacitor that allows for external biasing of transistor Q1. This capacitor is also used for input matching of the amplifier to a 50 ohm impedance. Temperature changes are very important for the stable operation of the amplifier, hence a special care has to be given to temperature stability. A bias circuit, in Figure 2, is designed for the stable operating temperatures between 23-40 ºC. It keeps the quiescent current constant, independent of temperature, by employing two diode connected transistors in series from the base of Q2 to the ground. The base biasing resistor (R4) is chosen to be approximately 10-15 times larger than 50 Ω to block the RF signal leakage that may cause a drop of output power and efficiency. By changing the V_{ref} control voltage, one can set the quiescent current precisely during test and measurement. The DC-feed inductor L_D is off-chip, to increase the efficiency of the power amplifier. If the reactance of this inductor is much higher than that of the output matching circuit, this inductor could be realized on-chip without sacrificing efficiency. This condition is successfully satisfied in designs with high frequency and high-power levels which require small output loads, leading to on-chip realization of the RF-choke inductor L_D. This is the main reason that the DC feeding inductor should be chosen as large as possible. Due to the potential usage of this PA in a fully-integrated transmitter, this inductor has to be designed on-chip and high value on-chip inductors have very low quality factors. In this work, special consideration is taken for the design of this inductor. C_2 is used for both DC-blocking and output matching purposes. Since in biomedical implantable electronic systems, the transmitted power is very low and the body significantly attenuates the high-frequency signals, the output filter could be avoided in order to improve the efficiency. Using the parasitic capacitance and inductance of the connection lines as part of the circuit elements, the passive component numbers were decreased, leading to an improvement in the efficiency.

The design of the PA started with selecting the appropriate transistor in IHPs technology library. IHPs SiGe:C standard HBT transistor has an f_{max} of 90 GHz, β of 190 and collector-emitter breakdown voltage of 4V, which is suitable for low-power, high-frequency circuit designs. The transistor gives the maximum β while it is driven by 20-50 μA base current, allowing the maximum f_T values. The required power levels are calculated to start the design from the output part of the circuit. Load-pull

simulations are performed for finding adequate impedance values to provide the maximum output power. Using Load-pull analysis results, the maximum achievable output power was also calculated and potential transistor sizes were selected. A single transistor with an effective emitter area of 21.6 μm^2 was selected as the optimum value. All the design parameters of the core PA circuit and the biasing circuit can be seen from Fig. 1 and Fig. 2.

III. LAYOUT CONSIDERATIONS

Design and simulation of the power amplifier were performed using Cadence® SpectreRF simulator and Agilent Design System (ADS)® environments, supported by the IHP technology library. The designed circuits were fabricated using IHP's SGB25VD technology. A die photo of the tested PA is shown Fig. 3; the layout occupies an area of approximately 1 x 0.5 mm^2. In order to decrease the resistance of the metallization lines, stacked metal layers were used. RC extraction was performed using the Assura® tool under Cadence® environment. All the inductors were re-modeled with stacked metal layers. Also, long paths were extracted as an inductor for increasing the accuracy of the post-layout simulations. Inductive extraction was performed using the Agilent ADS® MOMENTUM tool. Larger valued, bypass capacitors were used and are critical in order to reduce ground bounce and noise. Guard rings which are typically a square ring of substrate contacts or well trenches surrounding the active and passive devices, are also used in this work for improving the noise interference of the circuit. The collector and emitter paths of the transistor, which handle the DC and AC currents, were drawn with wider and stacked metals. Another important concept for high power RFIC design is grounding. Grounding of the circuit should be (close to) perfect at all the points on the integrated circuit. This is possible only if the ground plane of the PA is large enough. The free spaces of the layout are fully filled with a ground plane which prevents small voltage drops. All the capacitors used in the layout are M-I-M capacitors.

Low-power amplifiers generally suffer from lower efficiency performance. In particular Class-A and Class-AB operation mode power amplifiers have limited efficiency. As mentioned in the design part, the DC-feeding inductor has a large influence on efficiency of the amplifier due to its rather higher value (~8nH). The DC-feeding inductor was designed and optimized for 2.4 GHz operation. Stack metal layers were used in the realization of this inductor. Via sizes / numbers and underneath

metal width specifications were optimized. The **RF D**esign **E**nvironment (RFDE) tool is used for 2.5-D EM simulations which are integrated into the Cadence Virtuoso layout tool. The designed DC-feed inductor has a value of ~8nH and a maximum quality factor of over 20 at 2.4 GHz. The quality factor curves for this inductor are given in Figure 44. Inductors with different quality factor values were also simulated and the approximate efficiency curves were extracted. As seen in

Figure 5, the efficiency of the amplifier decreases from 32% to 25% for -5 dB input power which is very close to the input-referred compression point of the power amplifier. This optimization was performed with a 2 V supply voltage.

Figure 55 shows the importance of the DC-feeding inductor which was also used as a part of the output matching circuit. The efficiency of the power amplifier in a transmitter block is the most dominant factor of power consumption which in turn impacts on the means battery life.

IV. MEASUREMENT RESULTS

The measurements were performed using an Agilent 8719ES Network Analyzer, Karl-Suss RF Probe Station and a set of RF GSG probes. The gain of the amplifier with 2V supply voltage is over 12 dB over the 2 GHz to 2.4 GHz operating frequency range and can be seen in

Figure 6.

The input of the amplifier is also matched to 50-Ω. In Figure 7, the S_{11} performance of the amplifier with 2 V supply voltage, is given. As seen from Figure 77, the input is not fully matched but it is close to 50-Ω. The transmitter block was planned to be fully integrated and the preceding circuits's output impedance value may be easily matched to the input impedance of the power amplifier.

The output of the power amplifier is connected to an antenna which means the output value requires a 50-ohm impedance for maximum power transfer. As seen from Figure 88, the output of the circuit is well matched to 50-Ω between 2 GHz and 3 GHz with 2 V supply voltage.

For 1V low-power operation, all the S-parameter measurements were repeated and given in Figure 9, Figure 10 and Figure . As seen from Figures 9-11, the gain value decreased from 11 to 8 dB. The gain and the required output power strongly depend on the distance between transmitter and receiver. The designed power amplifier has the capability of working with both 2V and 1V supply voltages which gives flexibility to the transmitter block to operate in power-save mode. The input and output matching

performance of the circuit has not changed considerably due to the change of supply voltage.

The linearity performance of the circuit was measured with the same setup by sweeping the input power and monitoring the gain of the amplifier. Figure 22 shows that for 2V supply voltage operation mode, the power amplifier has an output-referred 1-dB compression point of 5.75 dBm. Figure 33 gives the 1-dB compression point performance of the power amplifier with 1V supply voltage. 1dBm output power is measured as the 1-dB compression point of PA using a 1 V low-supply voltage.

Table I shows our results and their comparison with similar ones available in the literature. As seen in Table I, our work can operate at the lowest supply voltage while still, being fully on-chip, giving competitive power gain and efficiency values, indicating the strength of the design methodology applied in this work.

V. CONCLUSION

We have designed, fabricated and characterized a fully-integrated, very-low power SiGe Power Amplifier (PA), realized for the 2.4 GHz ISM band using IHP (Innovations for High Performance), 0.25μm-SiGe process. The PA delivers an output power of 3.75 mW for a 2 Volt supply and 1.25 mW for a 1 Volt supply voltage. Measurements also yielded the following performance parameters of the PA; gain of 13 dB, 1-dB compression point of 5.7 dBm, and Power-Added-Efficiency of 30% for 2V supply voltage. For 1 Volt of supply voltage, the parameters are a gain of 10 dB, 1-dB compression point of 1 dBm, and Power-Added-Efficiency of 20%. In both supply voltage operations, the input and the output of the circuit give good reflection performance. With these performance parameters, the PA circuit, presented here, could be well-suited for low-power biomedical implanted transceiver systems.

ACKNOWLEDGMENT

W e thank the Scientific and Technological Research Council of Turkey (TUBITAK) for the financial support for this project under the contract number 107E014 and title “RF Transmitter–Based Transducer for Biosensor Applications.”

REFERENCES

[1]. S. C. Cripps, Advanced Techniques in RF Power Amplifier Design Norwood: Artech House, INC, 2002.

[2]. S.L. Chen, H.Y. Lee, C.A. Chen, H.Y. Huang, C.H. Luo; "Wireless sensor network system by separating control and data path (SCDP) for bio-medical applications" *Proceeding of European Microwave Conference 2007*, pp. 430-433, 8-12 October 2007, Munich Germany, ISBN: 978-2-87487-001-9, INSPEC Accession Number: 9831543

[3]. G. Ducar, P. Mingo and J. Valdovinos; "Predistortion Method for Nonlinear DistortionCancellation in WiMAX Transmitters" *Wireless Communication Systems*, 2006, pp. 786 – 790

[4]. K. Nellis and P.J. Zampardi; "Comparison of Linear Handset Power Amplifiers in Different Bipolar Technologies" *IEEE Journal of Solid-state Circuits*, vol. 39, pp. 1746-1754, Oct. 2004.

[5]. J. B. Johnson, A. J. Joseph, D.C. Sheridan, R. Maladi, P. Brandt, J. Persson, J. Andersson, A. Bjorneklett, U. Persson, F. Abasi,and L. Tilly "Silicon-Germanium BiCMOS HBT Technology for Wireless Power Amplifier Applications" *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1605-1614, Oct. 2004.

[6]. M. Helaoui, S. Boumaiza, A. Ghazel and Fadhel M. Ghannouchi, "On the RF/DSP Design for Efficiency of OFDM Transmitters " *IEEE Transaction on Microwave Theory and Techniques*, vol. 53, no. 7, July 2005, pp. 2355-2361.

[7]. Y. Ding and R. Harjani, "A high-efficiency CMOS 22 dBm linear power amplifier," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1895–1900, Sep. 2005.

[8]. P.B. Khannur, "A CMOS power amplifier with power control and T/R switch for 2.45-GHz Bluetooth/ISM band applications," *IEEE Radio Frequency Integ. Circuits Sym.,*pp. 145-8, June 2003.

[9]. IHP 0.25 µm SiGe:C BiCMOS with High-Voltage Devices Process Parameters, *http://www.ihp-microelectronics.com/16.0.html*

[10]. P.B. Khannur, "A CMOS power amplifier with power control and T/R switch for 2.45-GHz Bluetooth/ISM band applications," *IEEE Radio Frequency Integ. Circuits Sym.,*pp. 145-8, June 2003.

[11]. K. Yamamoto, T. Heima, A. Furukawa, M. Ono, Y. Hashizume, H. Komurasaki, S. Maeda, H. Sato and N. Kato, "A 2.4-GHz-band 1.8-V operation single-chip Si-CMOS T/R-MMIC front-end with a low insertion loss

switch," *IEEE Journal of Solid-State Circuits*, vol. 36 (8), pp. 1186-97, Aug. 2001.

[12]. Y. H. Chee, J. Rabaey and A. M. Niknejad, "A class A/B low power amplifier for wireless sensor networks," Proc. *IEEE Int. Sym. Circuits Systems*, vol. 4, pp. 409-412, May 2003.

[13]. M.M. El-Desouki, M. J. Deen, Y. M. Haddara, **"**A low-power CMOS class-E power amplifier for biotelemetry applications" *Proceeding 2005 European Microwave Week*, 3-7 October 2005, Paris, France, Volume 1, pp. 4-8, ISBN: 2-9600551-2-8

[14]. S. M. Abdelsayed, M. J. Deen, N. K. Nikolova **"**A fully integrated low-power CMOS power amplifier for biomedical applications" *Proceeding 2005 European Microwave Week*, 3-7 October 2005, Paris, France, Volume 3, pp. 1-4, ISBN: 2-9600551-2-8

[15]. A. Zolfaghari and B. Razavi, "A Low-Power 2.4-GHz Transmitter/Receiver CMOS IC," *IEEE Journal of Solid State Circuits*, vol. 38, no. 2, pp. 176-183, Feb. 2003.

[16]. K. Haridas, T. Hui, Yuan, Xiaojun; "A 2.4-GHz CMOS power amplifier design for low power wireless sensors network," *Radio-Frequency Integration Technology, RFIT 2009*. IEEE International Symposium on, pp.299-302, 9-11 Jan. 2009

FIGURE CAPTIONS

Figure 1: Single-Stage PA Schematic

Figure 2: Schematic of Bias Circuit

Figure 3: Chip Micrograph of the single-stage Power Amplifier

Figure 4: Quality Factor (Q) versus Frequency curve of the self-designed DC-feeding inductor

Figure 5: Efficiency versus input power with different quality factor values of DC-feeding inductor

Figure 6: S_{21} (V_{supply} = 2V) measurement result of the PA

Figure 7: S_{11} (V_{supply} = 2V) measurement result of the PA

Figure 8: S_{22} (V_{supply} = 2V) measurement result of the PA

Figure 9: S_{21} (V_{supply} = 1V) measurement result of the PA

Figure 10: S_{11} (V_{supply} = 1V) measurement result of the PA

Figure 11: S_{22} (V_{supply} = 1V) measurement result of the PA

Figure 22: 1-dB Compression point (V_{supply} = 2V) measurement result of the PA

Figure 33: 1-dB Compression point (V_{supply} = 1V) measurement result of the PA

TABLE CAPTIONS

TABLE I: Comparison of Power Amplifiers for Bio-Telemetry Applications

TABLE I: Comparison of Power Amplifiers for Bio-Telemetry Applications

Ref. #	Technology (μm)	Frequency (GHz)	PA Class	Supply Voltage (V)	P1dB (dBm)	Power Gain (dB)	PAE (%)	Integration Level
[10]	0.18CMOS	2.45	AB	1.8	3.5	13	14	On-chip
[11]	0.18CMOS	2.40	AB	1.8	9	19	16	Off-chip
[12]	0.13CMOS	1.92	AB	1.2	4	6	26	Off-chip
[13] filter	0.18CMOS	2.40	E	1.2	7	9	21	On-chip
[13] w/ofilter	0.18CMOS	2.40	E	1.2	9.5	11	33	On-chip
[14]	0.18CMOS	2.45	AB	1.4	6.5	19.5	28.5	On-chip
[15]	0.25CMOS	2.4	A	2.5	0	N/A	13.3	On-chip
[16]	0.18 CMOS	2.4	AB	1.8	6.4	11	18	On-chip
This Work	0.25BiCMOS	2.10-2.40	A	2	5.7	13	30	On-chip
				1	1	10	20	

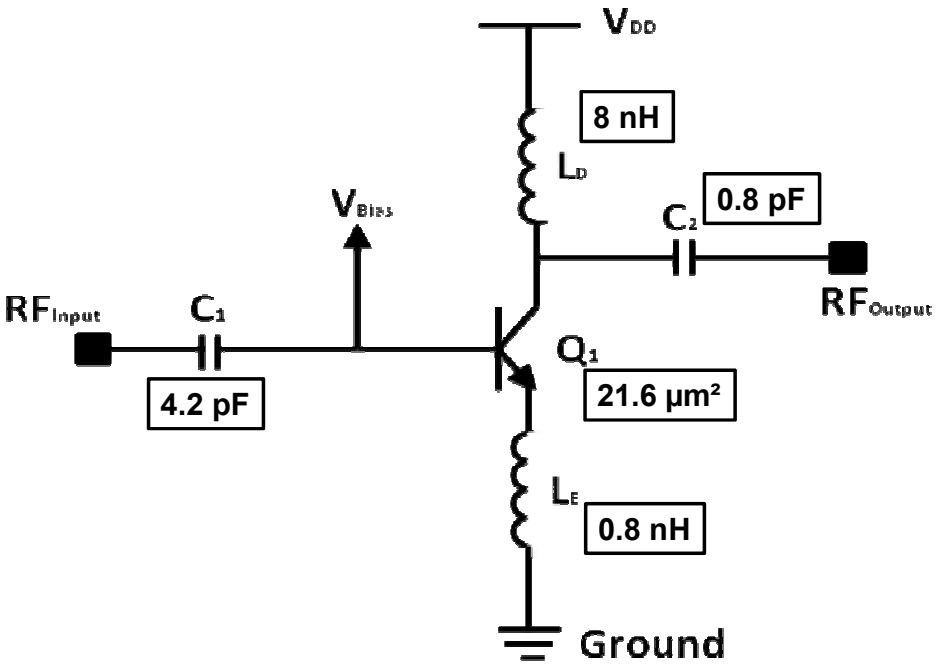

Figure 1: Single-Stage PA Schematic

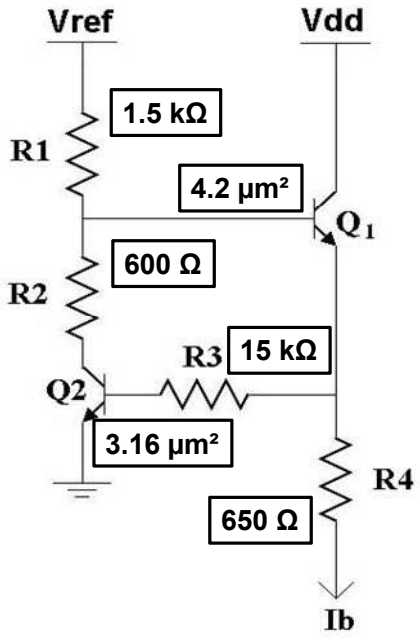

Figure 2: Schematic of Bias Circuit

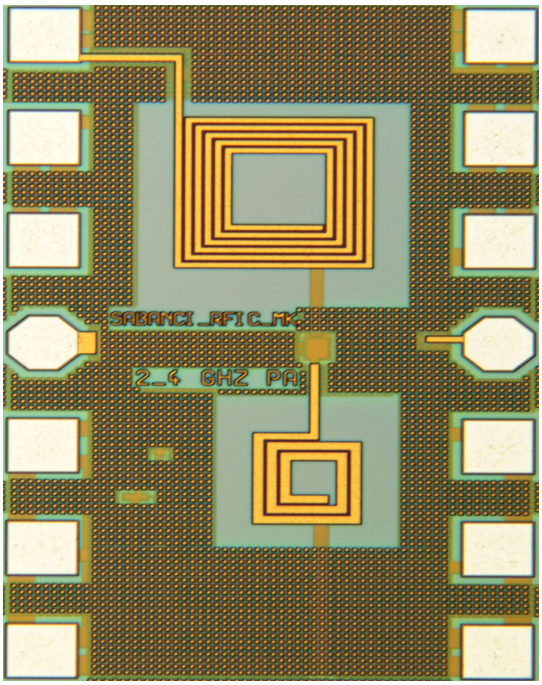

Figure 3: Chip Micrograph of the single-stage Power Amplifier

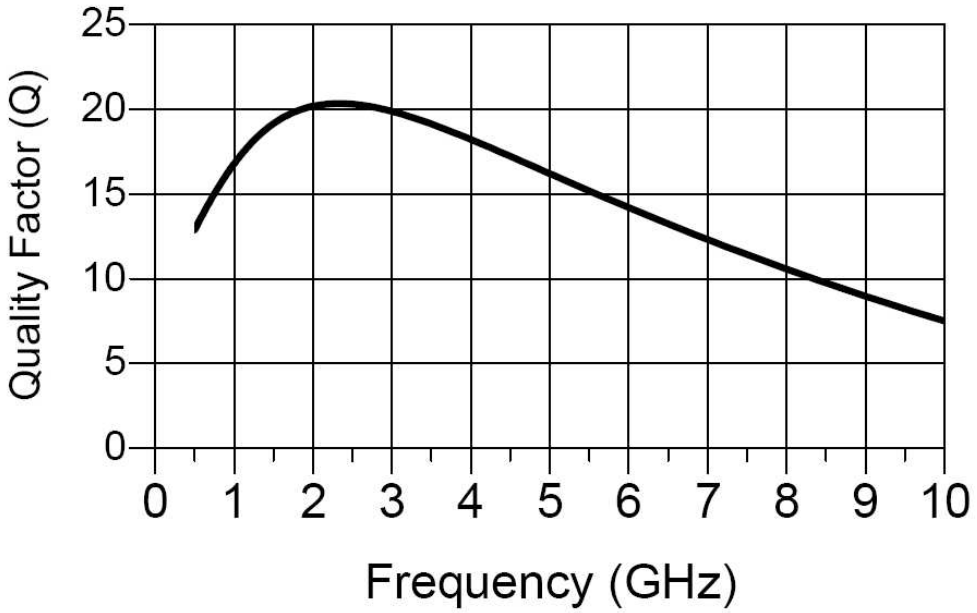

Figure 4: Quality Factor (Q) versus Frequency curve of the self-designed DC-feeding inductor

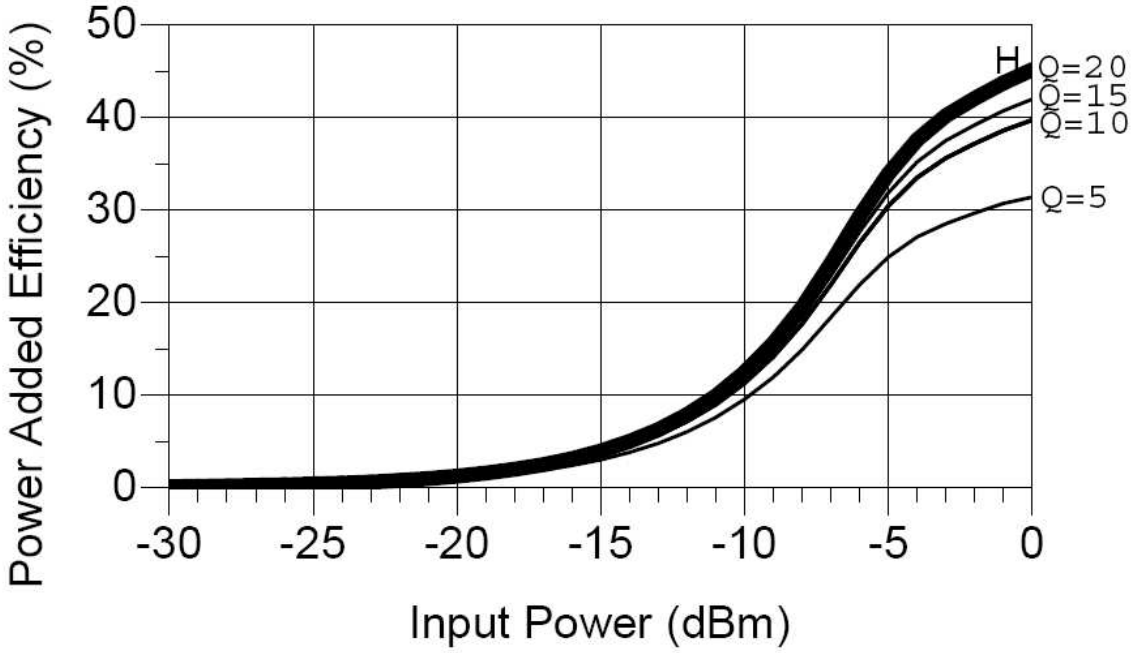

Figure 5: Efficiency versus input power with different quality factor values of DC-feeding inductor

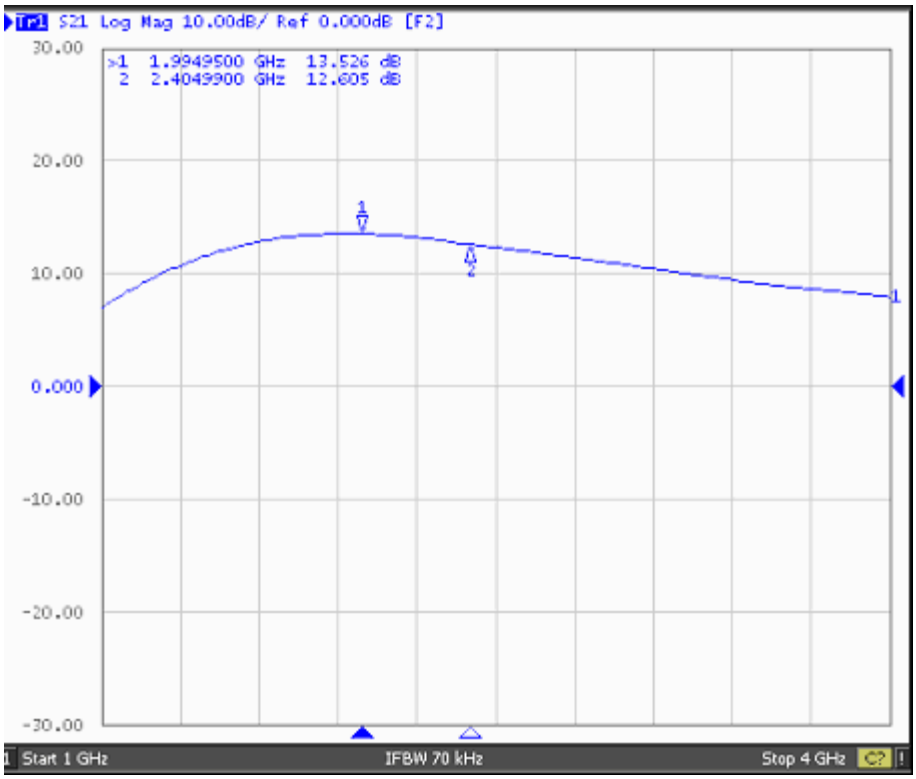

Figure 6: S_{21} (V_{supply} = 2V) measurement result of the PA

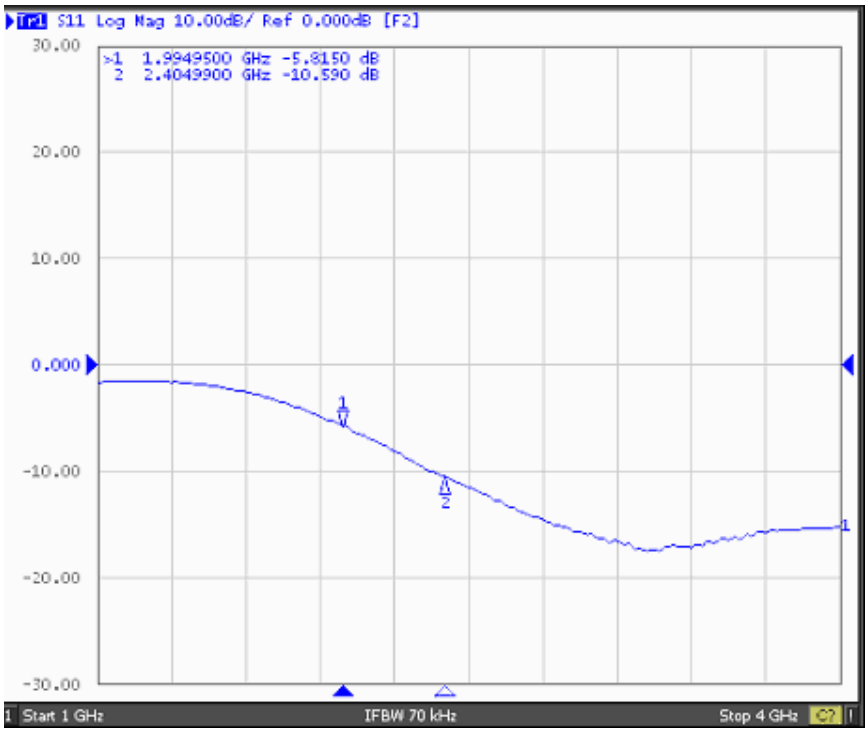

Figure 7: S_{11} (V_{supply} = 2V) measurement result of the PA

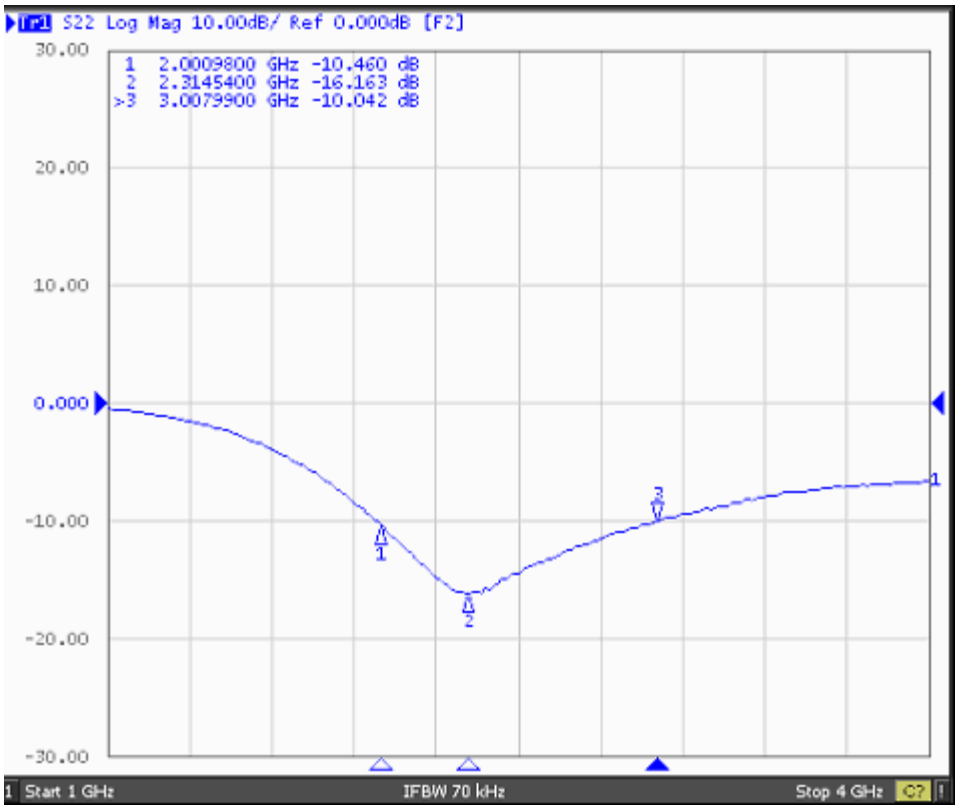

Figure 8: S_{22} (V_{supply} = 2V) measurement result of the PA

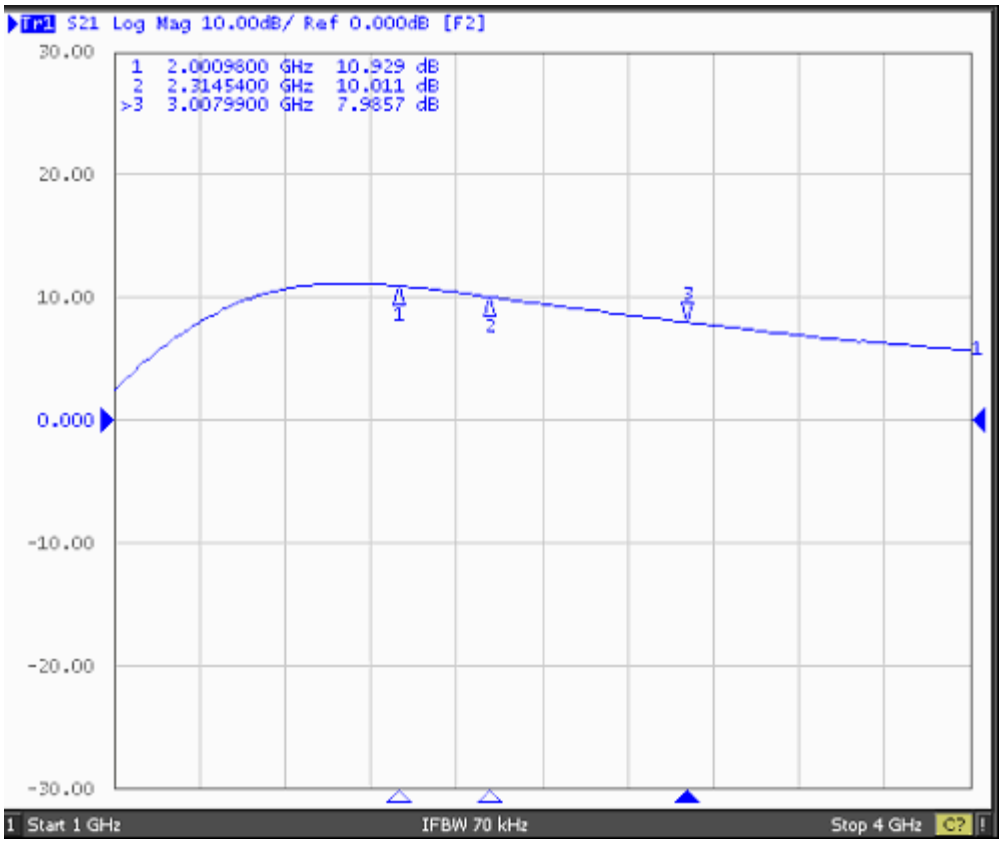

Figure 9: S_{21} (V_{supply} = 1V) measurement result of the PA

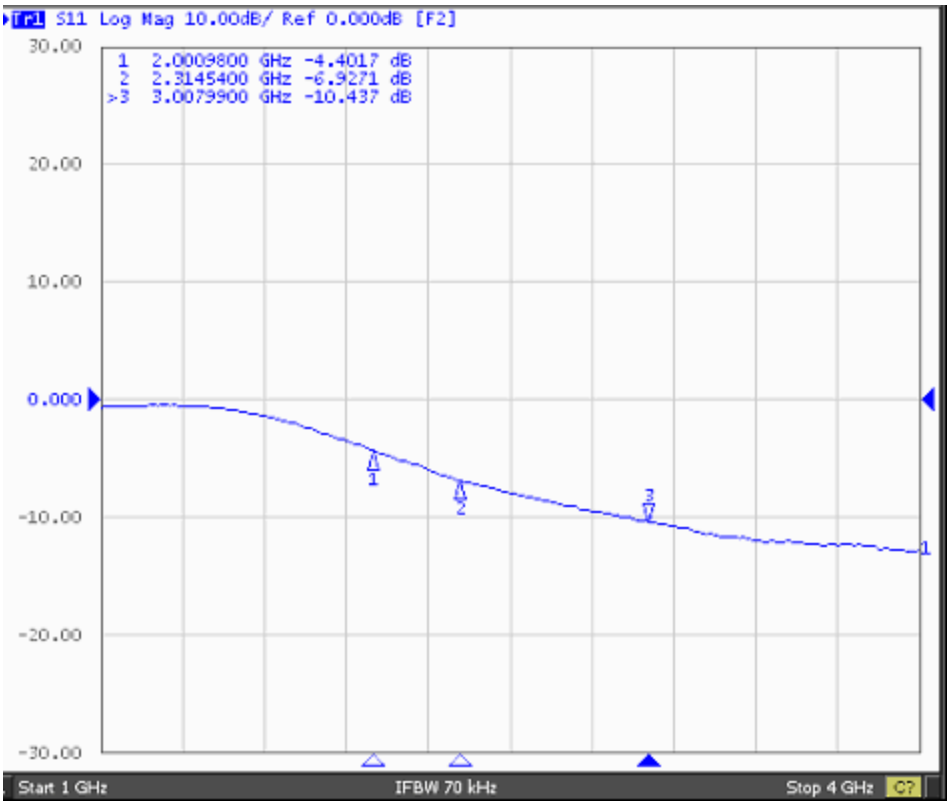

Figure 10: S_{11} (V_{supply} = 1V) measurement result of the PA

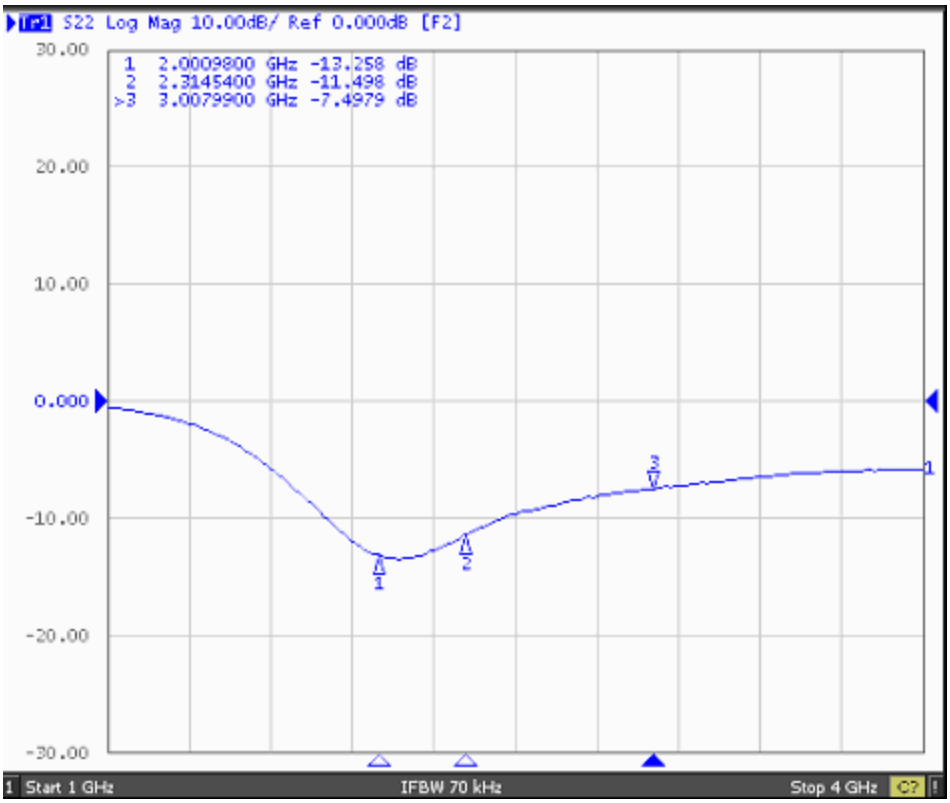

Figure 11: S_{22} (V_{supply} = 1V) measurement result of the PA

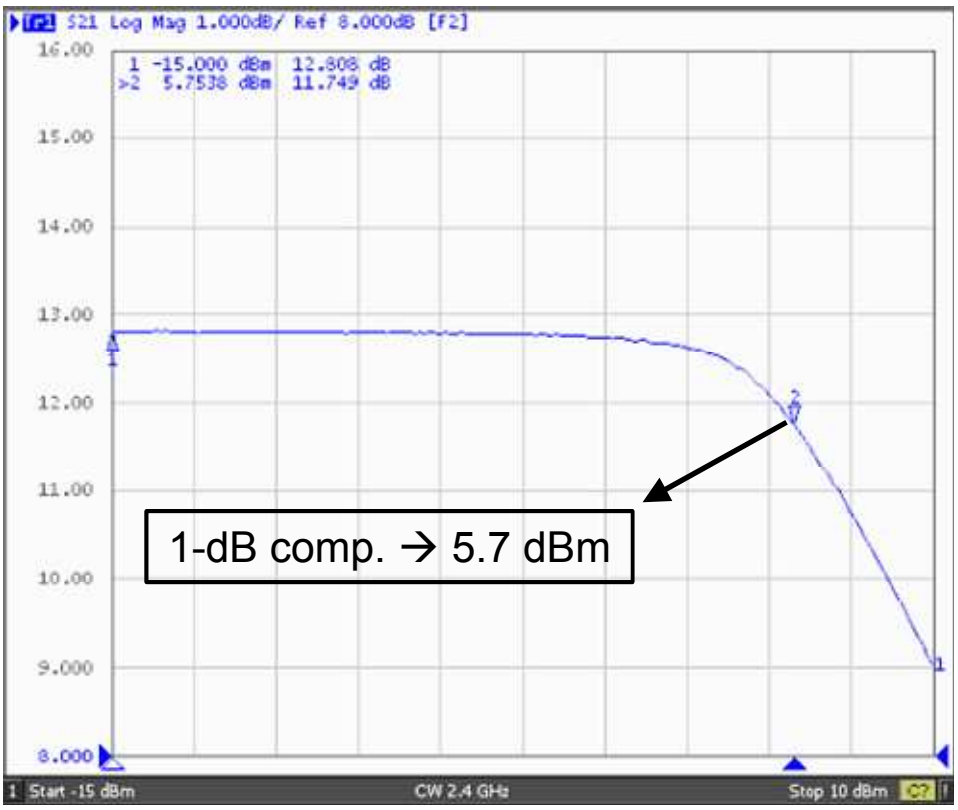

Figure 22: 1-dB Compression point (V_{supply} = 2V) measurement result of the PA

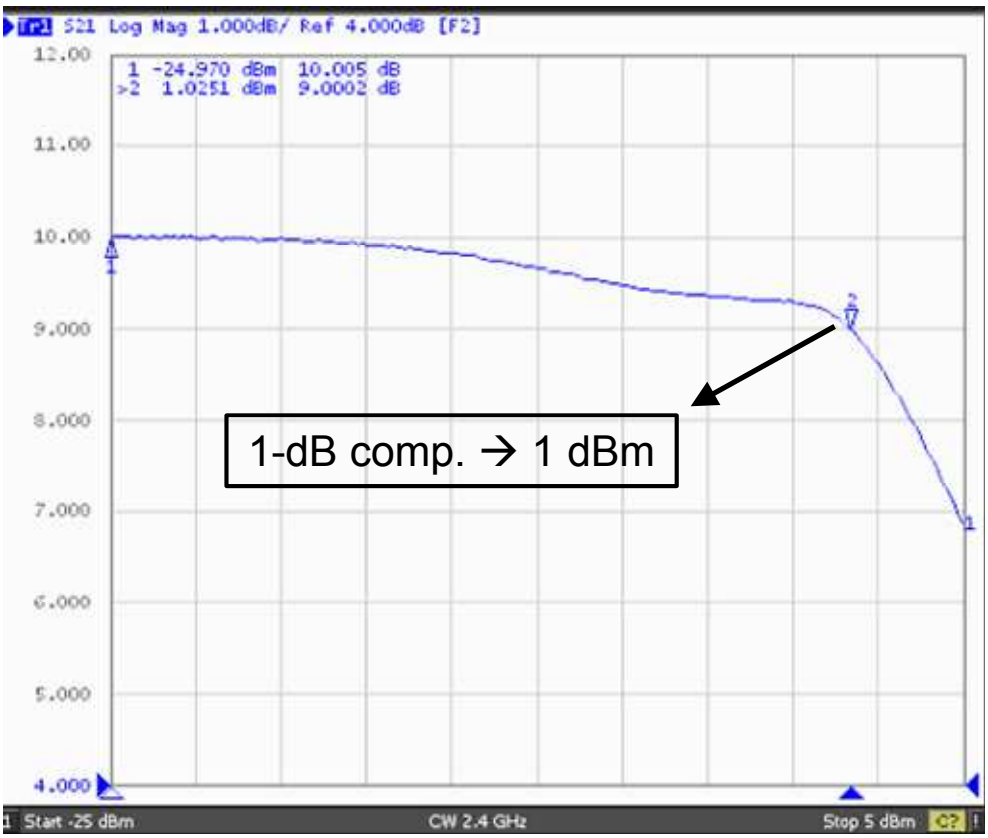

Figure 33: 1-dB Compression point (V_{supply} = 1V) measurement result of the PA